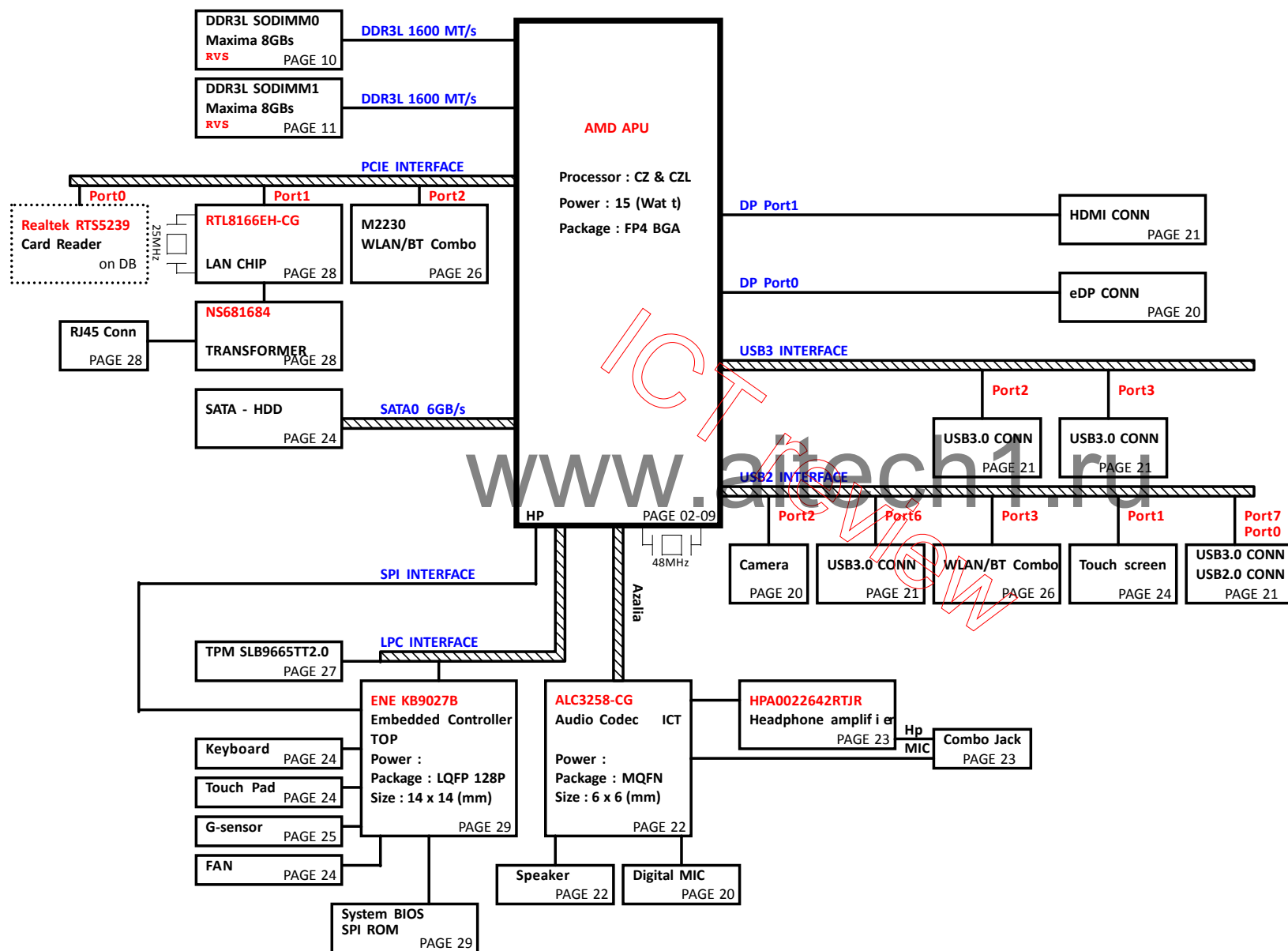


Dessert AMD CZ & CZL UMA 14"



PCB 6L STACK UP

LAYER 1 : TOP
LAYER 2 : SGND
LAYER 3 : IN1
LAYER 4 : IN2
LAYER 5 : SVCC
LAYER 6 : BOT

Power Source

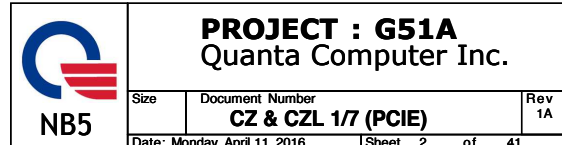
ISL88750 System Charge Power (+BATCHG) PAGE 31
SY8208B/SY8286C System Power (+3VPCU/+5VPCU/+3VSS/+5VSS) PAGE 32
RT8231B System Memory Power (+1.2VSUS/+0.6V_DDR_VTT/+2.5VSUS) PAGE 33
APW8826/APW8826/G9336 Processor Power (+0.95VS5/1.5VS5/0.775VS5) PAGE 34
AOZ1267/RT8068AZQW Processor Power (+0.95V/+1.8VS5) PAGE 35
ISL62771 Processor Power (+VCC_CORE/+VDDNB_CORE) PAGE 36.37
ISL62771 Processor Power (+APU_VDDGFX) PAGE 38.39
APL3523A *3 System Power (+3/+3VLAVCC/+5V/+3VSUS/ +1.5V/+1.8V_ROM/+1.8V) PAGE 40
G5018 Processor Power (+VDDCR_FCH_S5) PAGE 41

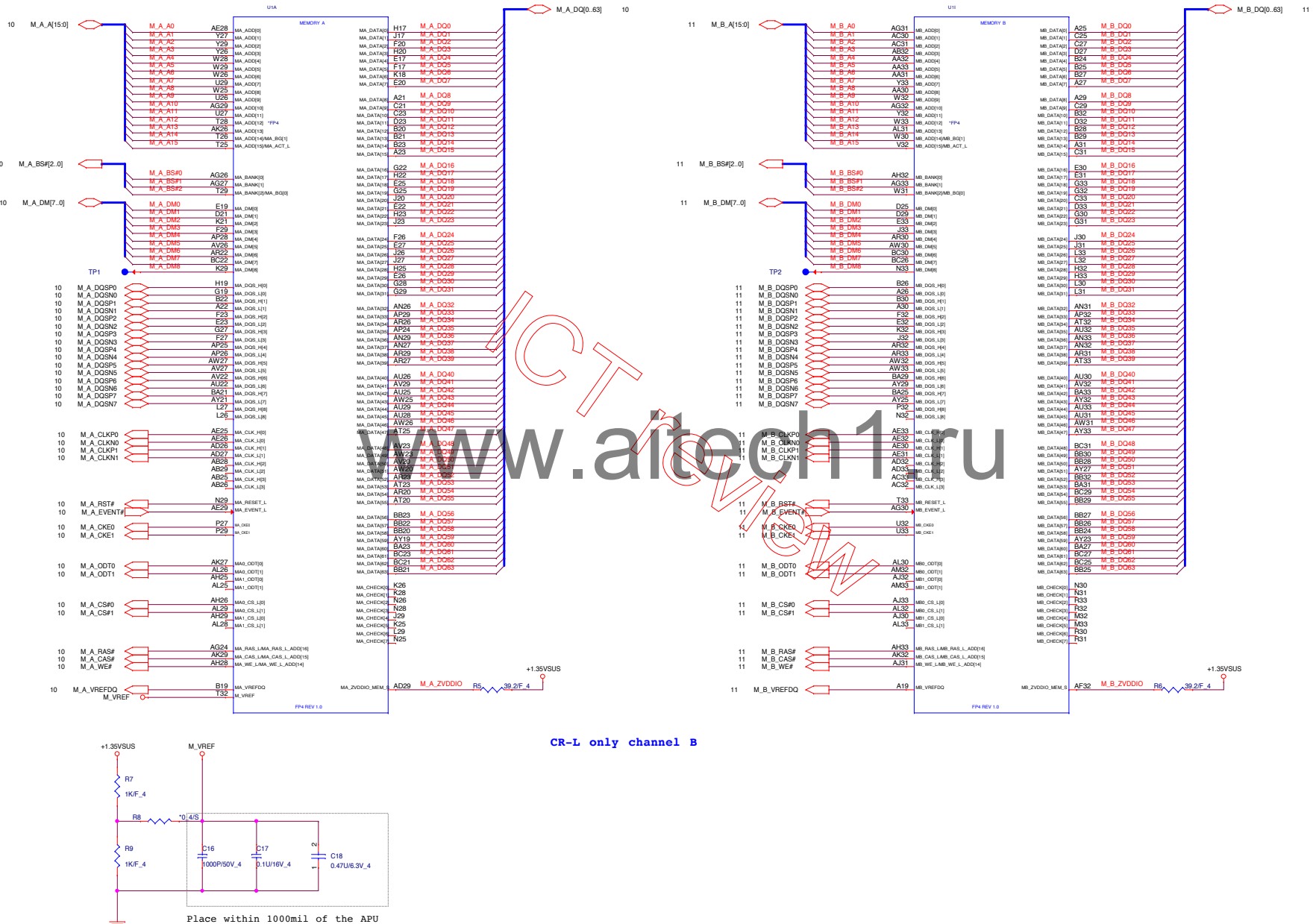


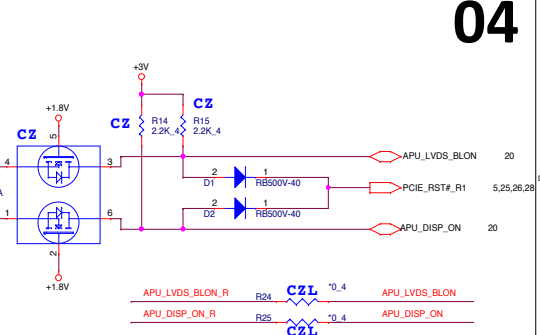
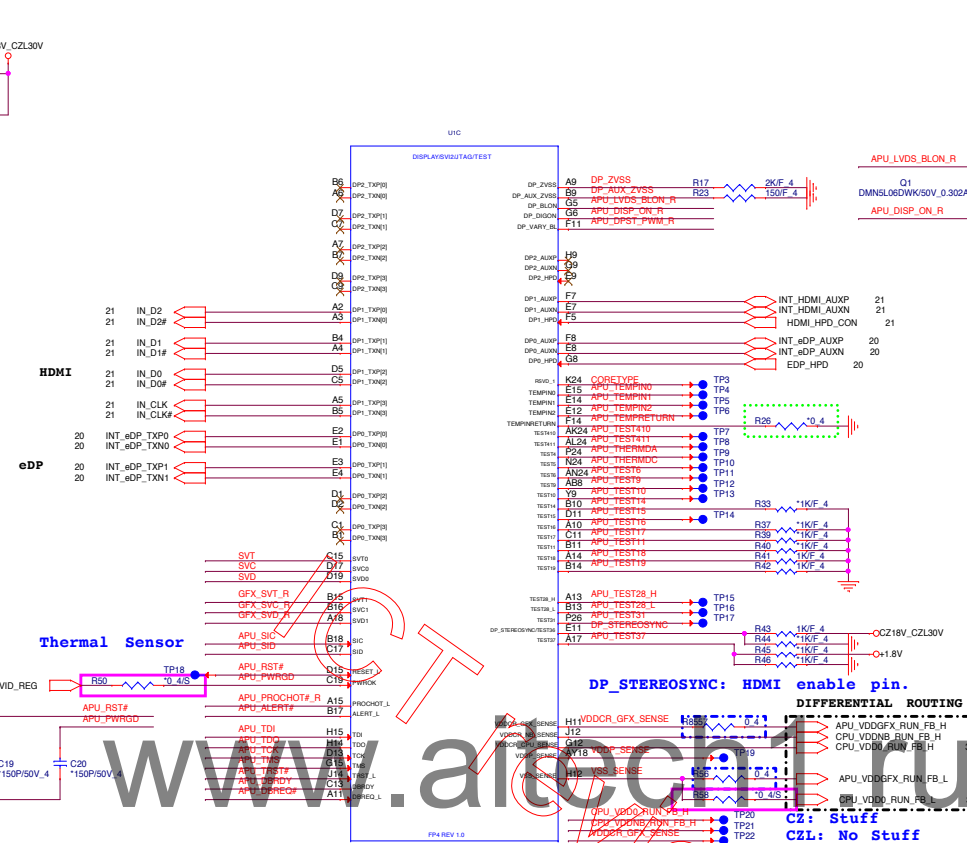
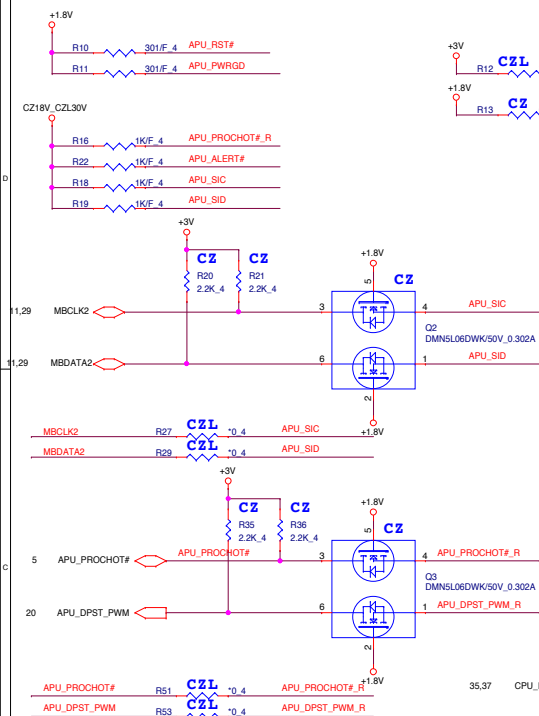
PROJECT : G51A
Quanta Computer Inc.

Size	Document Number	Rev
	Block Diagram	1A
Date: Monday, April 11, 2016	Sheet	1 of 41

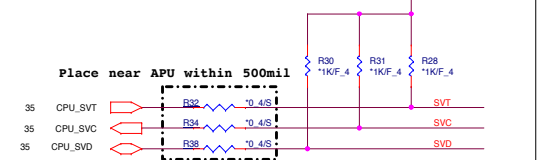
5	4	3	2	1	Дата: Monday, April 11, 2016	Sheet 2	91	41
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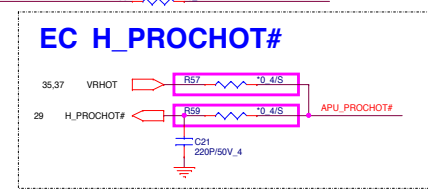
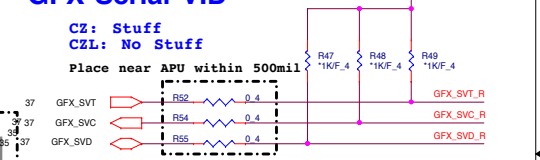




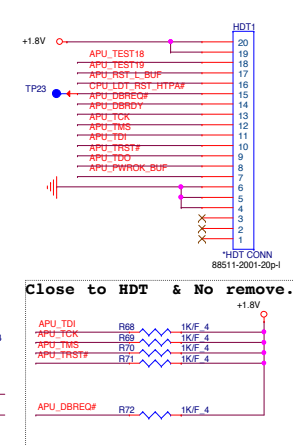
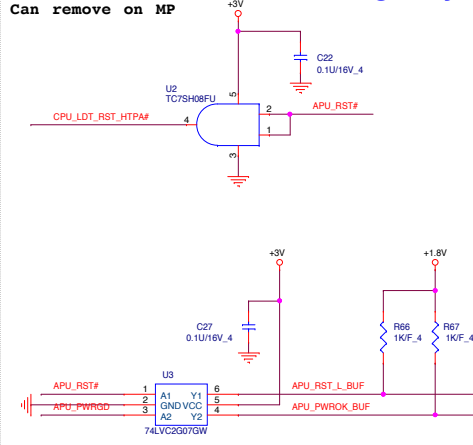
APU Serial VID



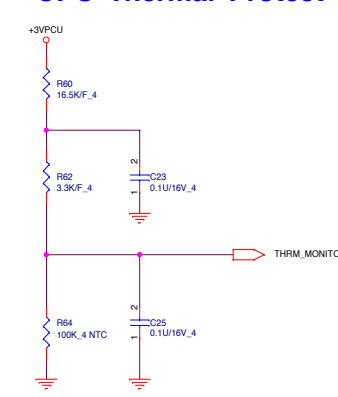
GFX Serial VID



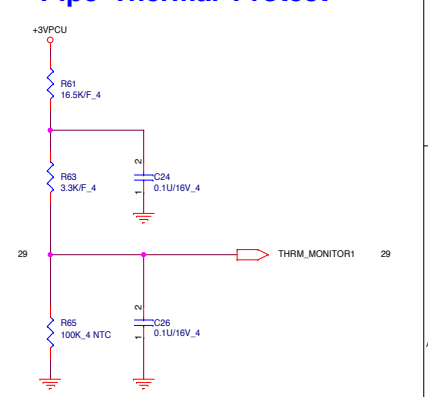
HDT+ Connector for Debug only



CPU Thermal Protec



Pipe Thermal Protect



Board ID 0	Definition
0	UMA
1	DIS

Board ID [2:1]	Definition
00	14 "
01	15 "
10	17 "
11	Reserve

Board ID [4:3]	Definition
00	Pavilion
01	Reserve
10	Reserve
11	Reserve

Board ID [5]	Definition
0/1	Reserve

Board ID [6]	Definition
0/1	Reserve

Board ID [7]	Definition
0/1	Reserve

t 53537_1_09 suggestion.

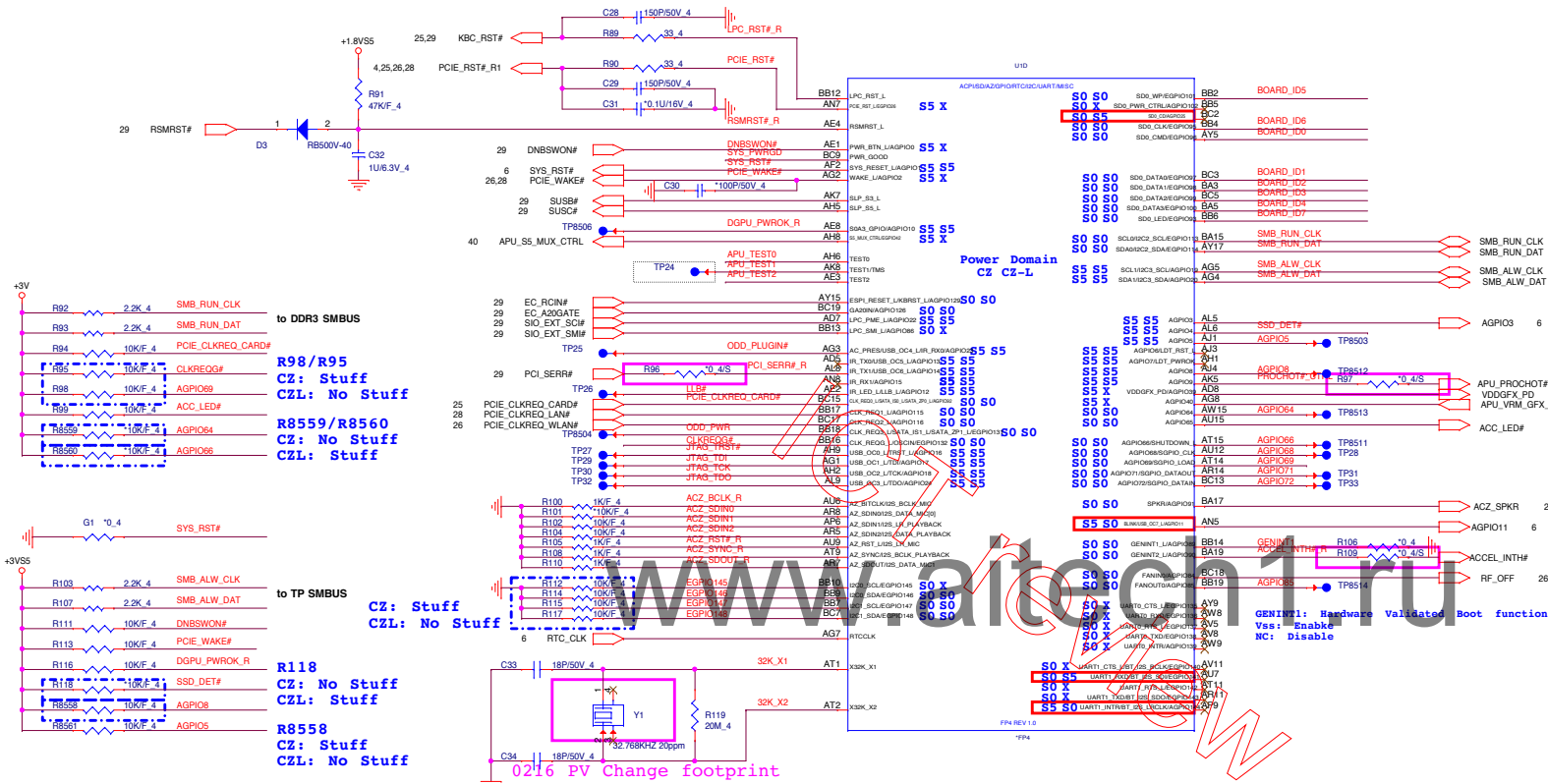


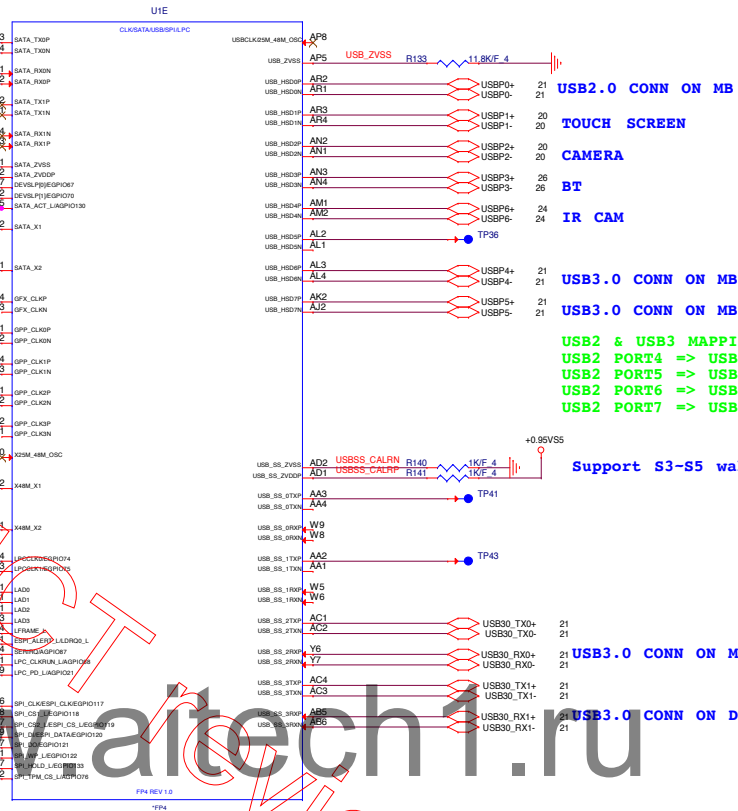
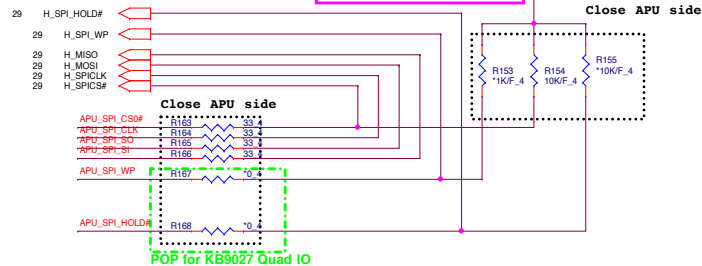
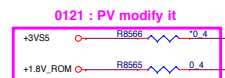
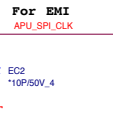
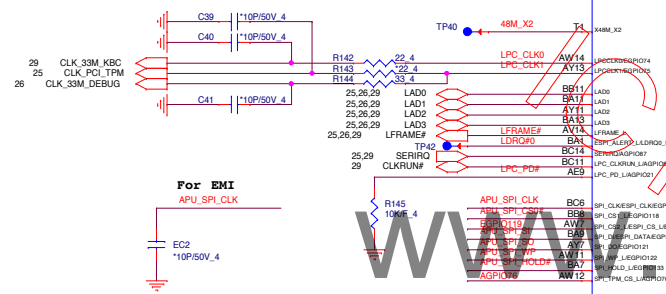
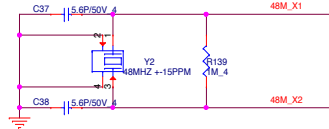
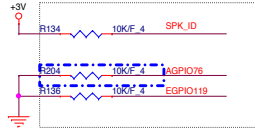
Figure 10 shows the ACZ pin connections. The connections are as follows:

- ACZ_SDOUT_AUDIO (Pin 22) is connected to R126 (33 ohms) and then to ACZ_SDOUT_R.
- ACZ_SYNC_AUDIO (Pin 22) is connected to R127 (33 ohms) and then to ACZ_SYNC_R.
- BIT_CLK_AUDIO (Pin 22) is connected to R128 (33 ohms) and then to ACZ_BCLK_R.
- ACZ_RST#_AUDIO (Pin 22) is connected to R129 (33 ohms) and then to ACZ_RST#_R.
- ACZ_SDI#0 (Pin 22) is connected to EC1 (10P50V) and then to ACZ_SDI#0.



TEST2	TEST1	TEST0	Description
0	0	0	FCH TAP accessible from APU when TAPEN is asserted FCH JTAP pins are overloaded for multiple functions, in this configuration the FCH JTAP are used as non-JTAP pins
0	0	1	Reserved
0	1	X	Reserved
1	TMS	0	FCH JTAP multi-function pins are configured as JTAP pins, in this configuration the FCH TAP can be accessed from FCH JTAP pins
1	TMS	1	Use on ATE only Yuba JTAP enabled

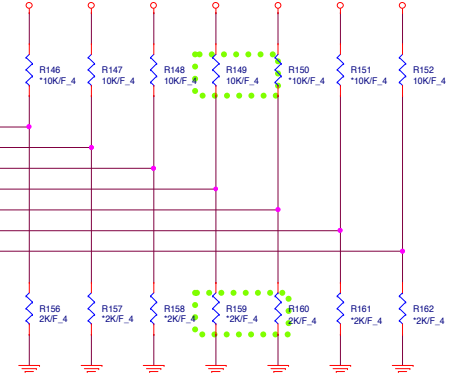
Follow Checklist



Support S3-S5 wake up

21 **USB3.0 CONN ON MB**
24

21 USB3.0 CONN ON DB



STRAPS PINS

OVERLAP COMMON PADS WHERE POSSIBLE FOR DUAL-OP RESISTORS.

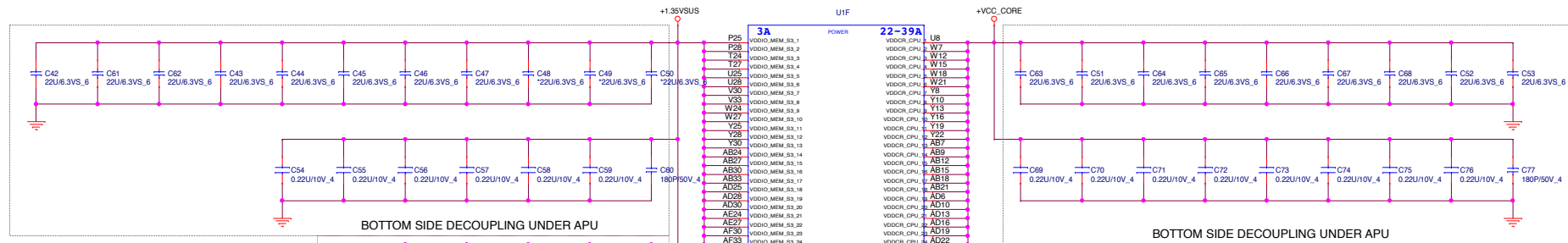
REQUIRED STRAPS

	LPC_CLK0	LPC_CLK1	LFRAME#	AGPIO3 int. Pull-Up	RTC_CLK int. Pull-Up	AGPIO11=BLINK int. Pull-Up	SYS_RST# int. Pull-Up
PULL HIGH	BOOT FAIL TIMER ENABLED	Use 48MHz crystal clock and generate both internal and external clocks DEFAULT	SPI ROM DEFAULT	CZ-L DEFAULT	CZ DEFAULT	Com battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to Fads. DEFAULT
PULL LOW	BOOT FAIL TIMER DISABLED DEFAULT	Use 100MHz PCIE clock as reference clock and generate internal clocks only DEFAULT	LPC ROM	3.3V SPI ROM DEFAULT	Default to traditional reset logic DEFAULT	Com battery is not on board. DEFAULT	LDT_RST#/LDT_PWRGD output to Fads DEFAULT

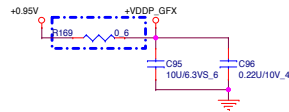


PROJECT : G51A
Quanta Computer Inc.

Size	Document Number CZ & CZL 5/7(SATA/USB/SPI)	Rev 1A
Date: Monday, April 11, 2016	Sheet	6 of 41

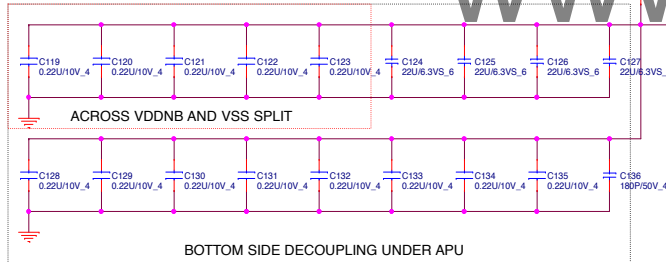
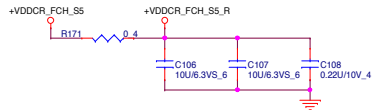


CZ: Always Stuff
CZL: DIS Stuff
UMA No Stuff

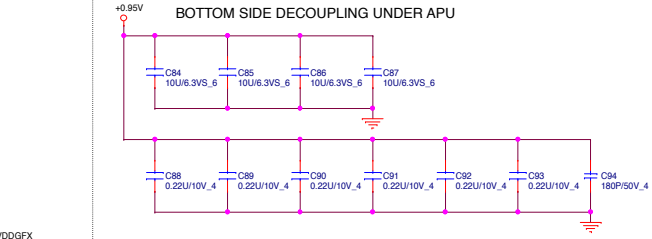
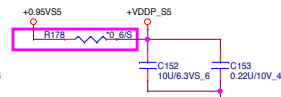
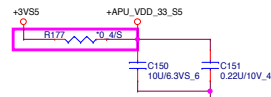
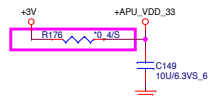
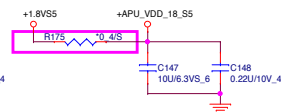
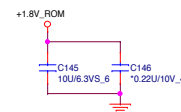
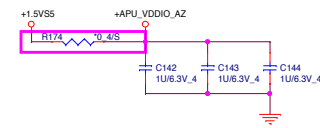


Only Stuff: CZL UMA

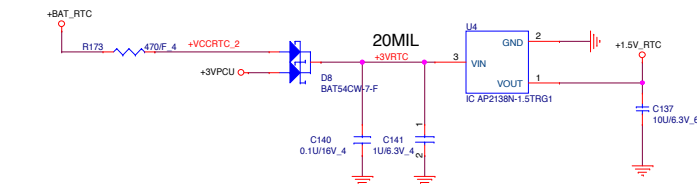
+VDDCR_FCH_S5
R171
CZ: Stuff
CZ-L: No Stuff



1.5V For HDA Only

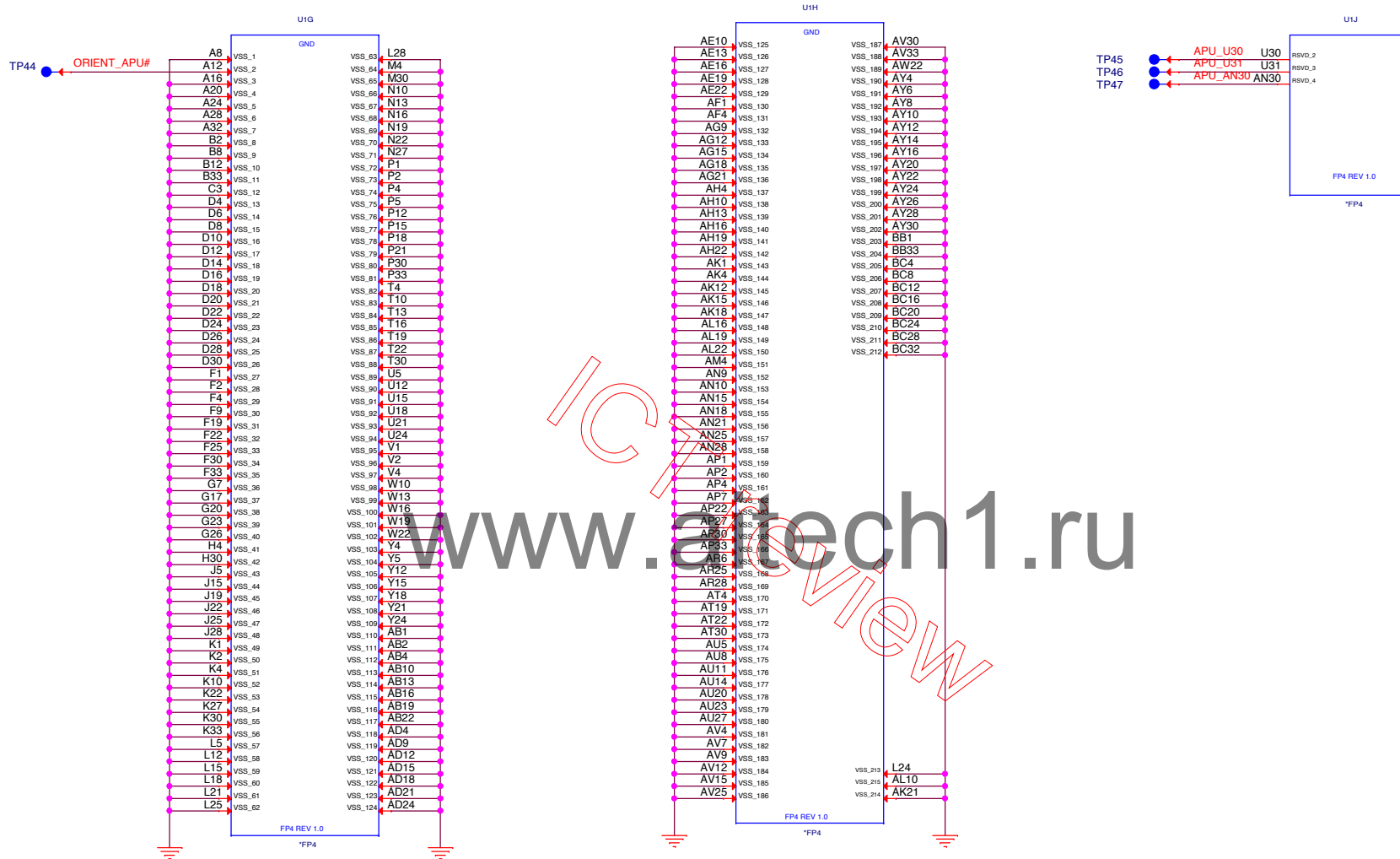


CZ: R11 +APU VDDGFX_RUN cap Stuff.
CZ-L: R11 +APU VDDGFX_RUN cap No Stuff.



PROJECT : G51A
Quanta Computer Inc.


Size	Document Number	Rev
NB5	CZ & CZL 6/7 (POWER)	1A
Date: Monday, April 11, 2016	Sheet	7 of 41

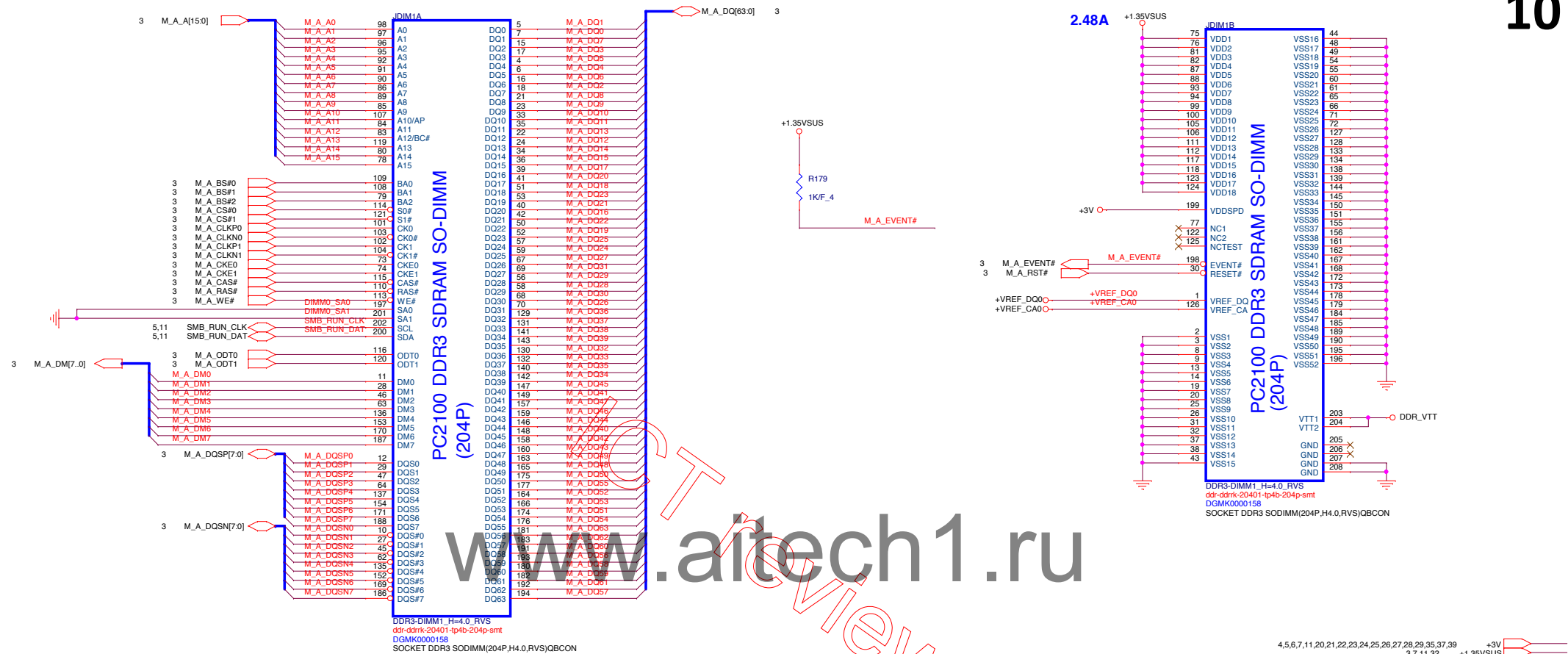


PROJECT : G51A
Quanta Computer Inc.

Size	Document Number	Rev
	CZ & CZL 7/7 (GND)	1A
Date: Monday, April 11, 2016 Sheet 8 of 41		

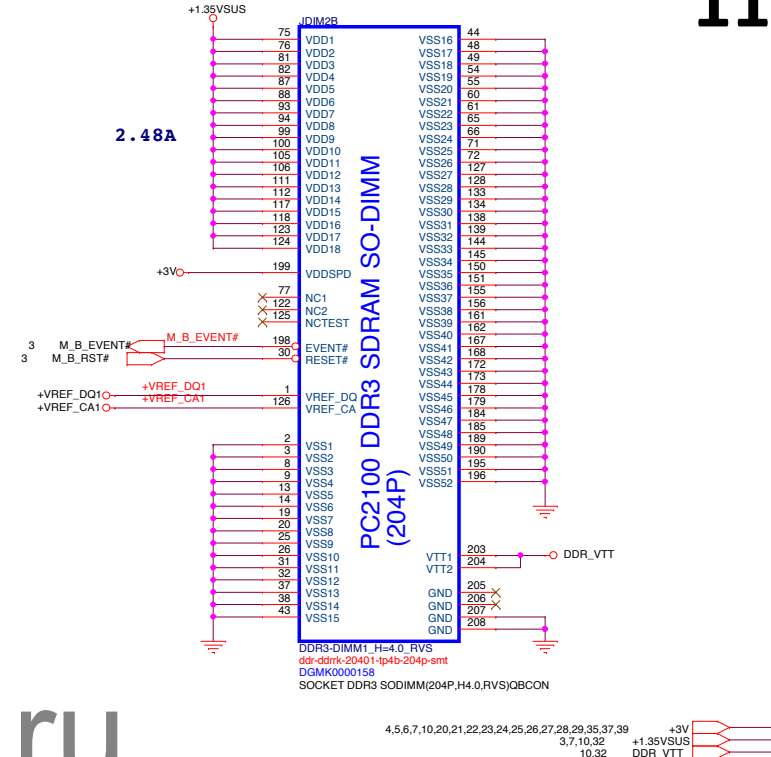
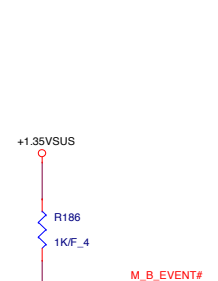
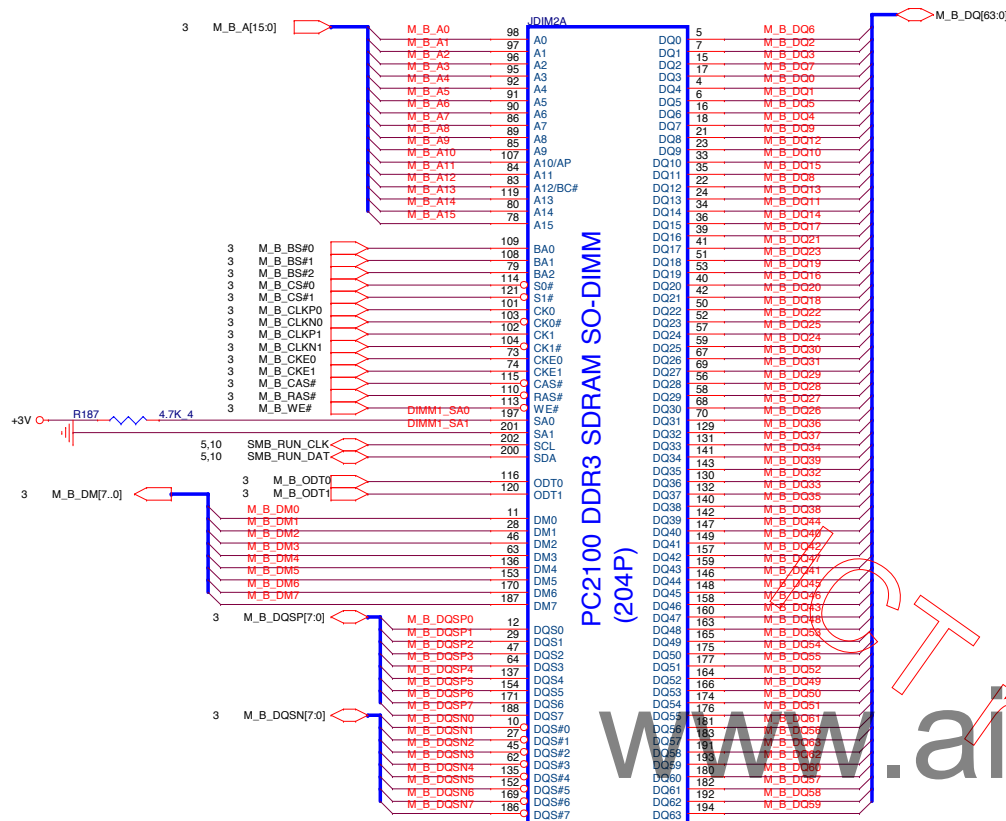
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www.aitech1.ru

 NB5	PROJECT : G51A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, April 11, 2016		Sheet 9 of 41



PROJECT : G51A
Quanta Computer Inc.

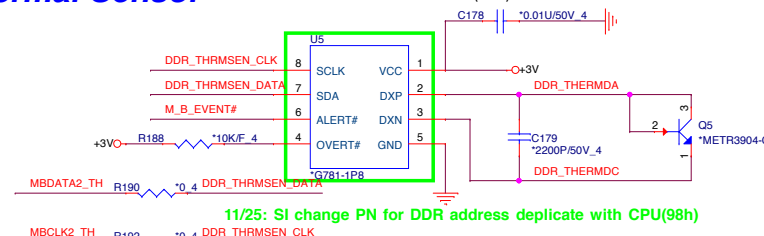
Size	Document Number	Rev
Custom	System Memory 1/2 (4H)	1A
Date: Monday, April 11, 2016	Sheet 1001	41



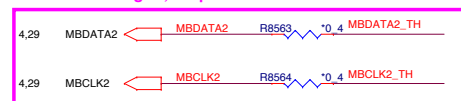
Local Thermal Sensor

DDR3 Thermal Sensor

Main:AL000781039 G781-1P8(9Ah)



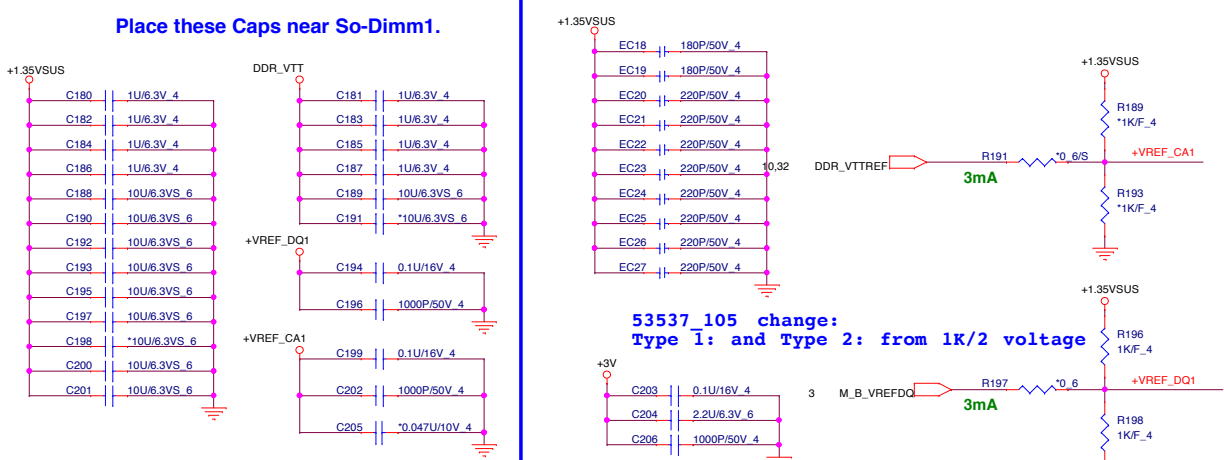
11/25: break length , all platform can not use it




Main:AL000781039 G781-1P8(9Ah)
2nd:AL001412005 EMC1412-2-ACZL-TR(9Ah)
Main:AL001412003 EMC1412-1-ACZL-TR(98h)
2nd:AL000431014 TMP431ADGKR(98h)

NB5		PROJECT : G51A Quanta Computer Inc.	
Size	Custom	Document Number	System Memory 2/2 (4H)
Date: Monday, April 11, 2016	Sheet	11of	41


Place these Caps near So-Dimm1.




<Reserved>
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 NB5	PROJECT : G51A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, April 11, 2016 Sheet 12 of 41		


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		PROJECT : G51A Quanta Computer Inc.	
		Size A Document Number Reserved	Rev 1A ICT
Date: Monday, April 11, 2016		Sheet	13 of 41


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 NB5	PROJECT : G51A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, April 11, 2016		Sheet 14 of 41


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 <p>NB5</p>		<p>PROJECT : G51A Quanta Computer Inc.</p>	
		<p>Size A</p>	<p>Document Number Reserved</p>
<p>Date: Monday, April 11, 2016</p>		<p>Sheet 15 of 41</p>	<p>Rev 1A</p>


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	PROJECT : G51A Quanta Computer Inc.		
	Size A	Document Number Reserved	Rev 1A
	Date: Monday, April 11, 2016 Sheet 16 of 41		

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www.aitech1.ru

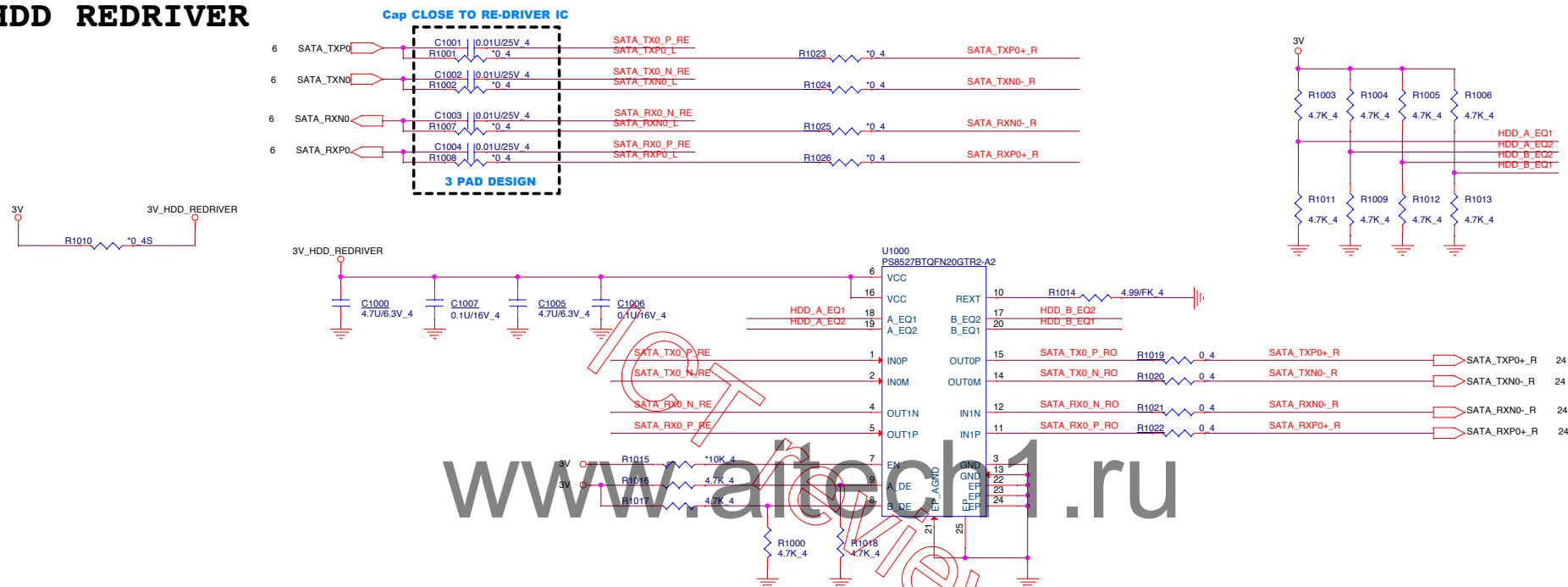
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		Size A	Document Number Reserved
Date: Monday, April 11, 2016		Sheet 17 of 41	Rev 1A

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www.aitech1.ru

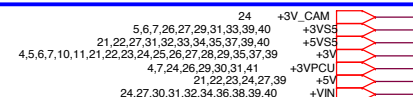
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	Size A	Document Number Reserved	Rev 1A
	Date: Monday, April 11, 2016		Sheet 18 of 41

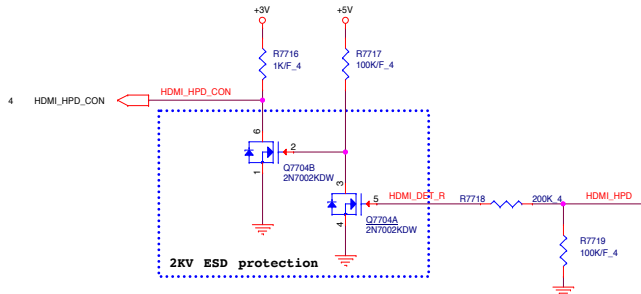
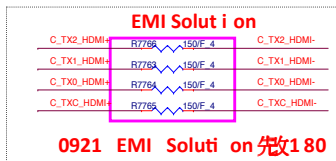
0407 : MV modify it

HDD REDRIVER



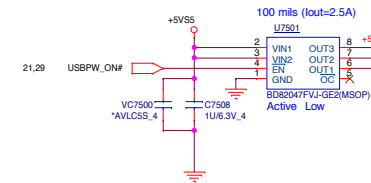
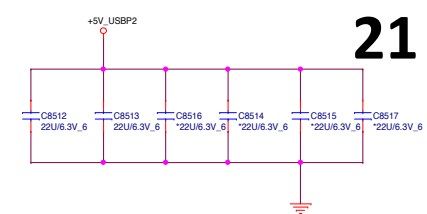
eDP Conn. 20





4,5,6,7,10,11,20,22,23,24,25,26,27,28,29,35,37,39
20,22,23,24,27,39
22,27,31,32,33,34,35,37,39,40

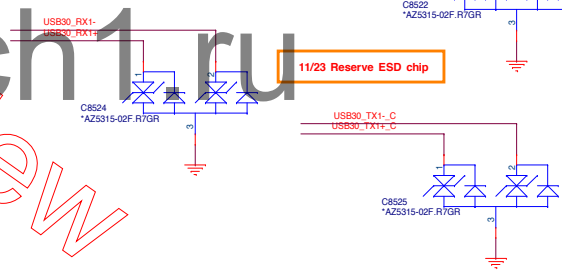
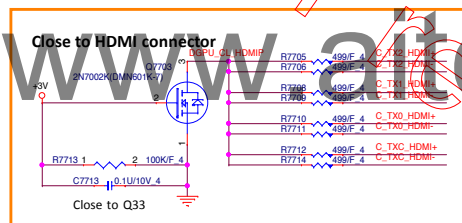
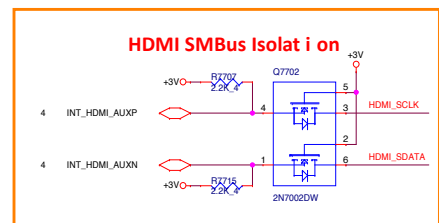
+3V
+5V
+5V5
+5V55



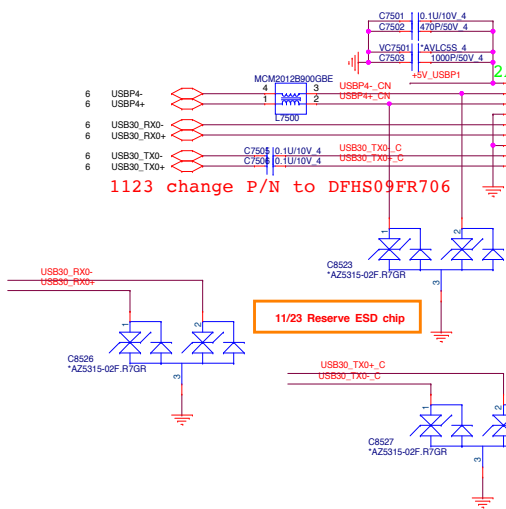
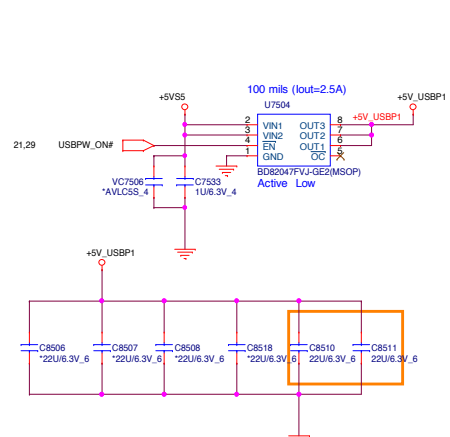
0216 PV Change footprint

USB 3.0

1123 change P/N to DFHS09FR706



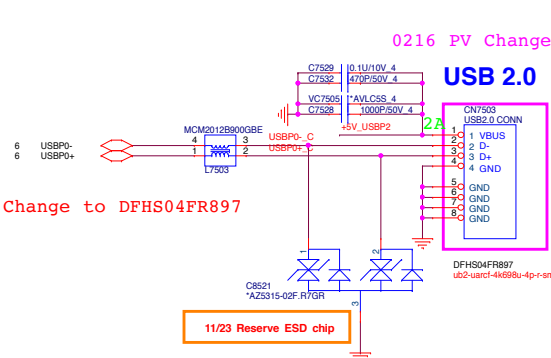
USB 2.0/3.0 Combo



USB 3.0

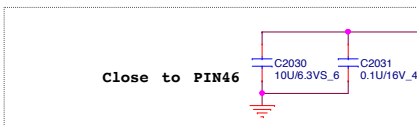
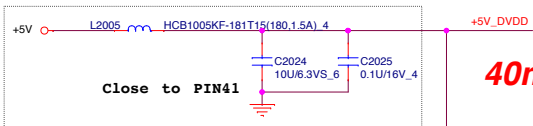
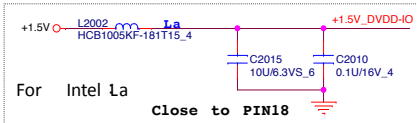
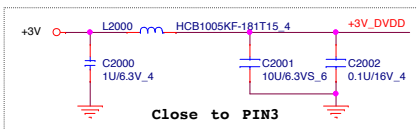
0216 PV Change footprint

1123 Change to DFHS04FR897

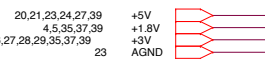
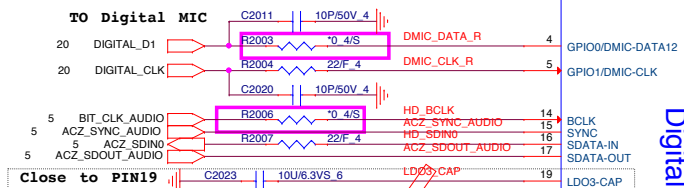


0216 PV Change footprint

USB 2.0

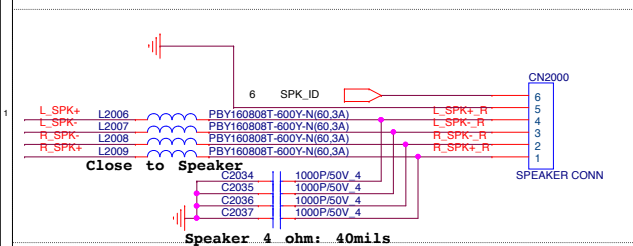
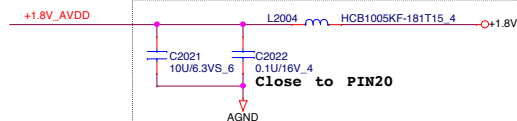
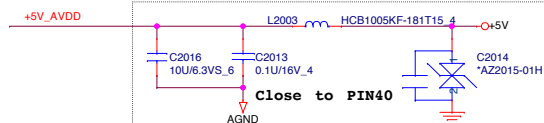


40mil



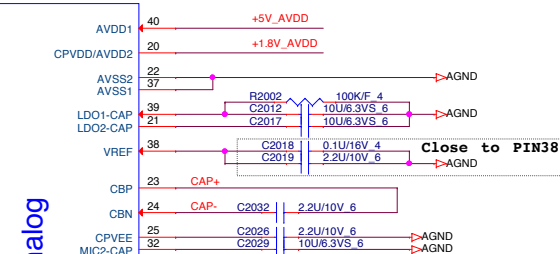
40mil

+5V_AVDD >40mils trace

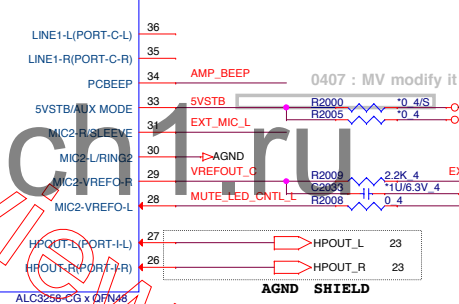


Speaker 4 ohm: 40mils

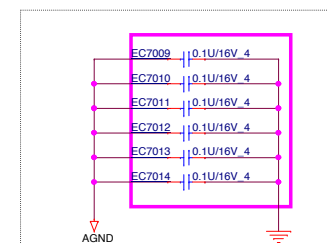
www.atech1.ru



Analog

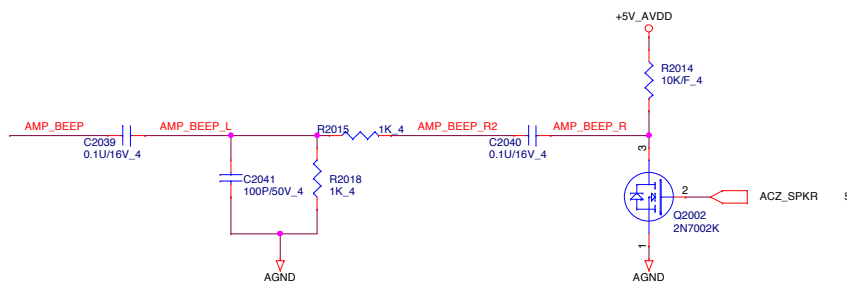
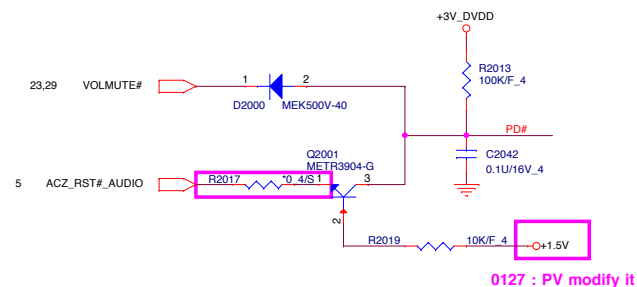


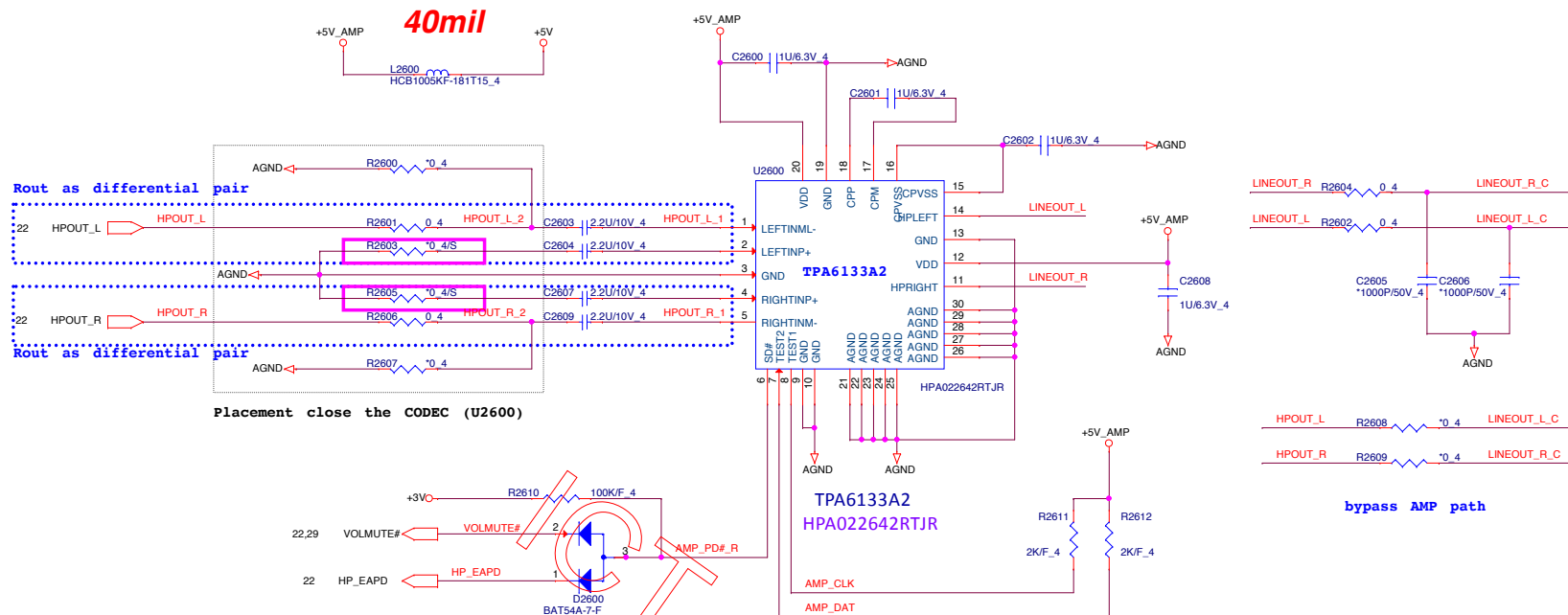
0215 : PV modify it



0218 : PV modify it from EMI request

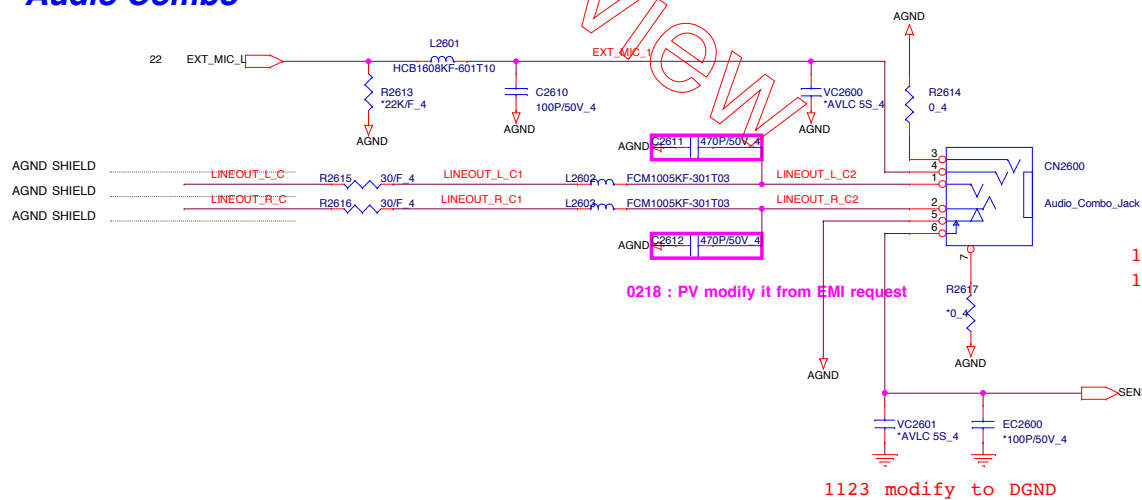
place to near or under codec

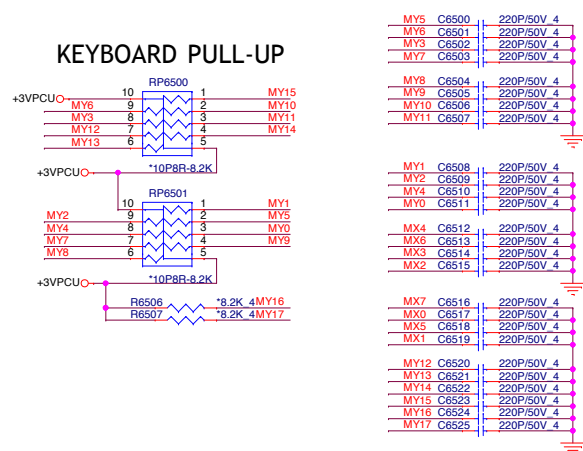
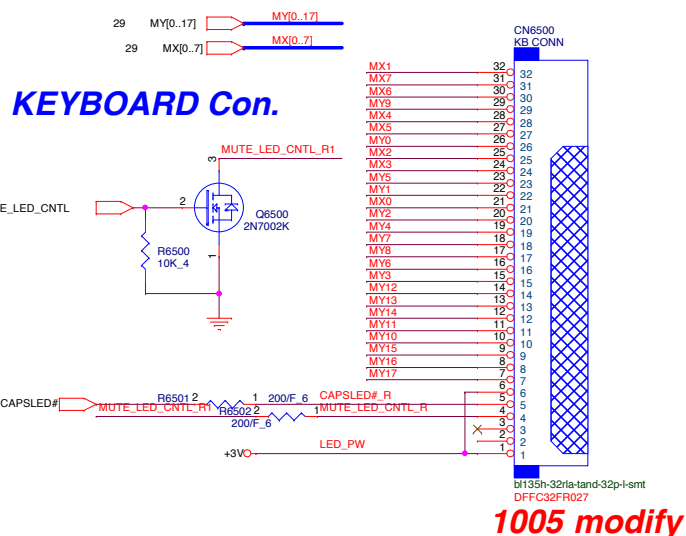




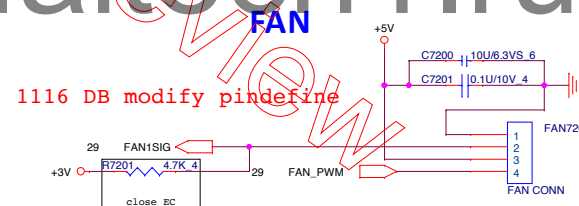
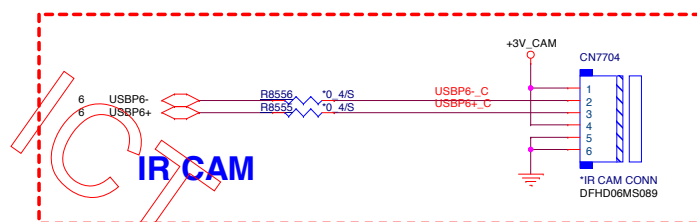
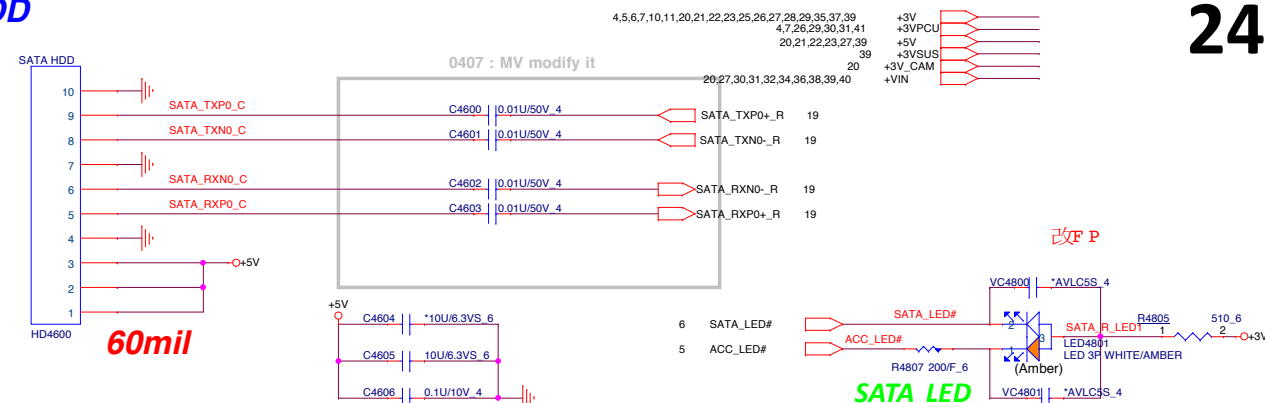
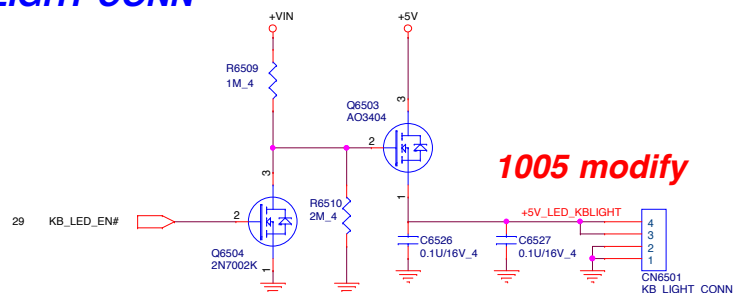
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Audio Combo

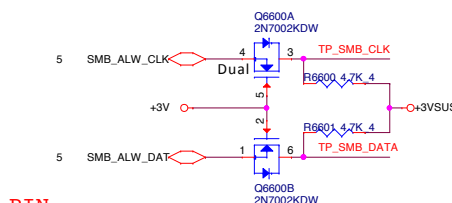
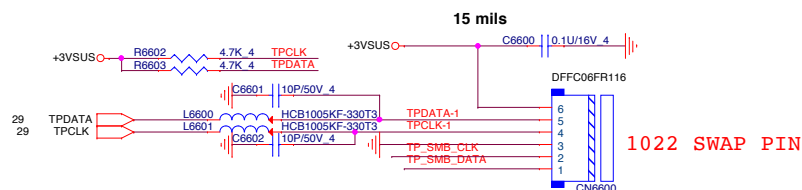




KB LIGHT CONN

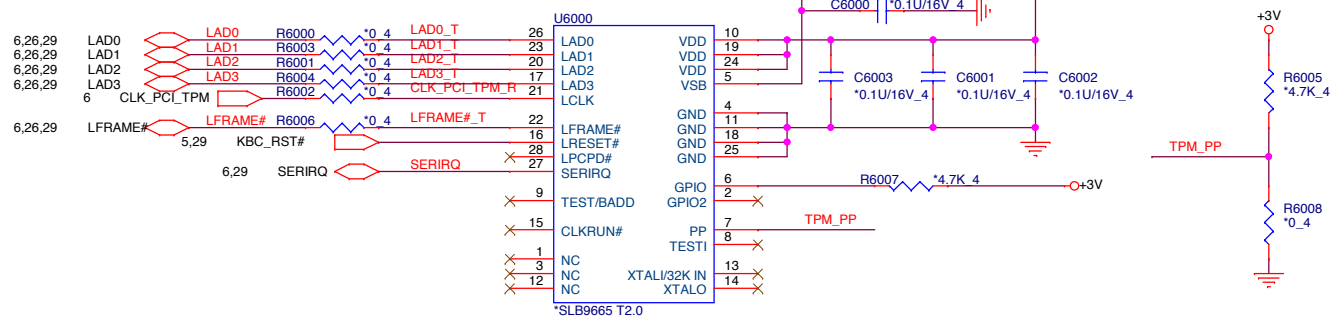


Touch Pad Connector

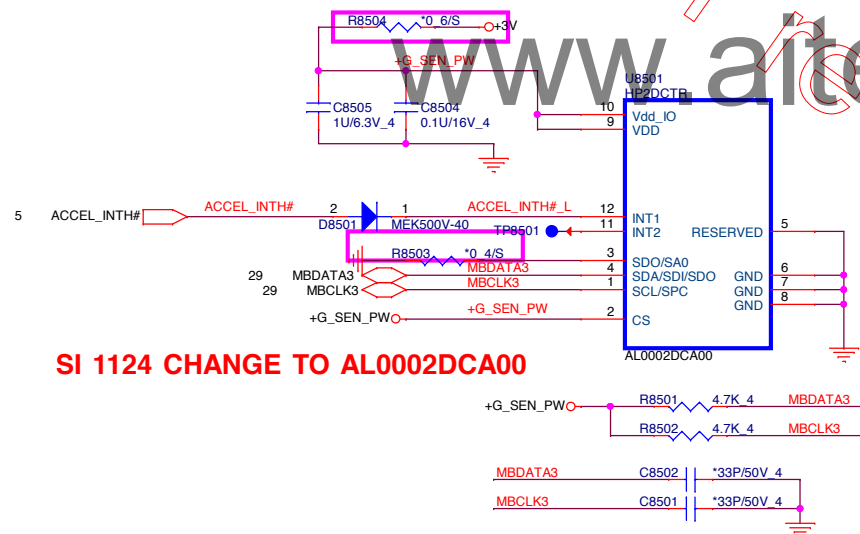


TPM (2.0)

PN:AL009665K01

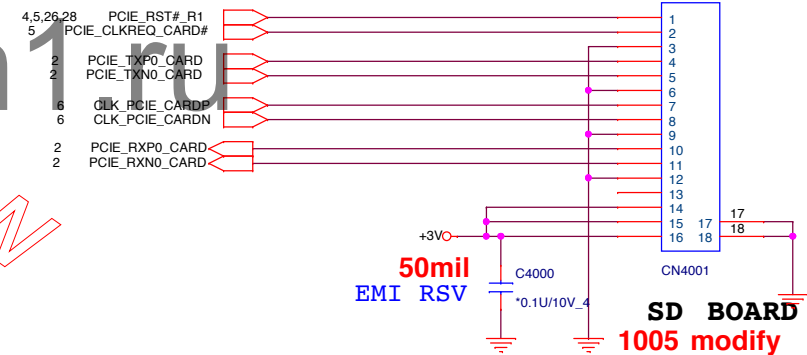


Accelerometer Sensor

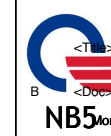


SI 1124 CHANGE TO AL0002DCA00

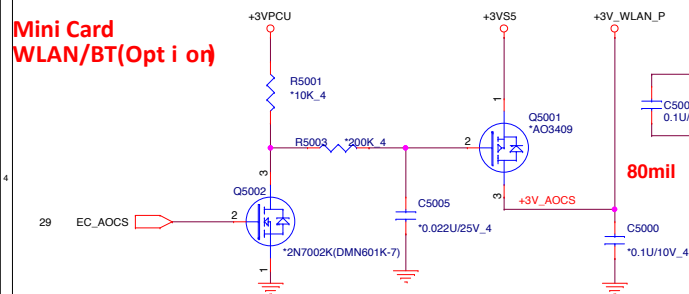
1014 modify pindefine

51619-01601-v01-16p-I
DFFC16FR04250mil
EMI RSVSD BOARD
1005 modify

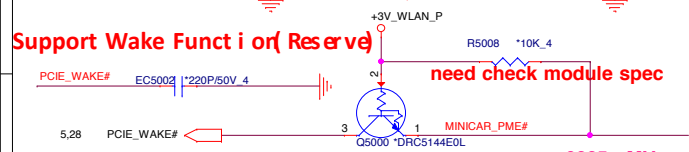
4,5,6,7,10,11,20,21,22,23,24,26,27,28,29,35,37,39 +3V

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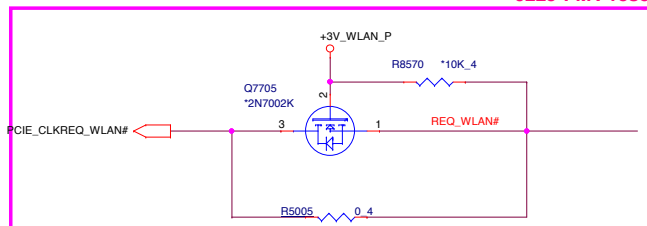
Size	Document Number	Revision
NB5	Monday, April 11 2016	25 41
Date:	Sheet	of

Mini Card
WLAN/BT(Optional)

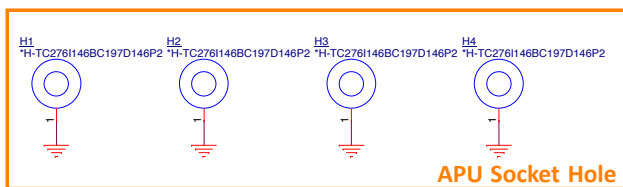
Support Wake Function (Reserved)



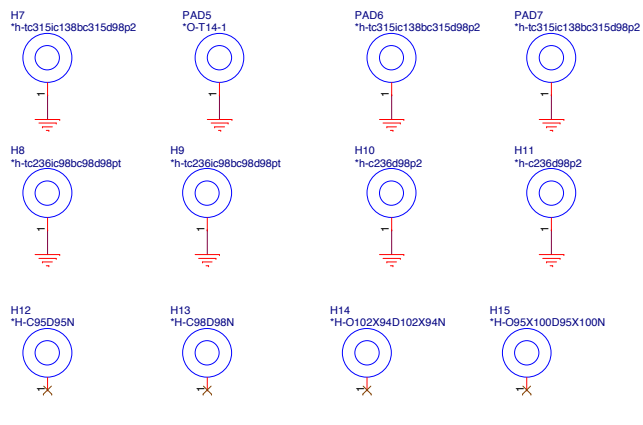
0225 : MV reserve for WLAN card level shift



PAD/HOLE



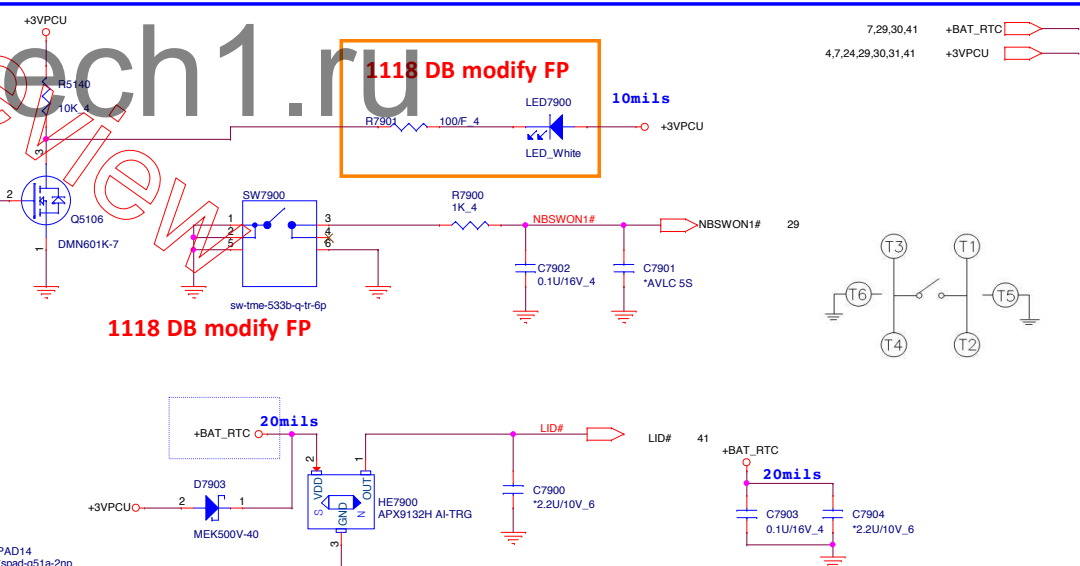
APU Socket Hole



1118 change to M2 MBZRQ001010

Add for EMI

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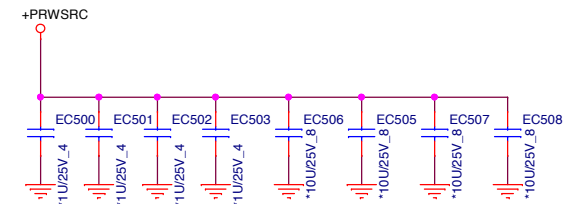
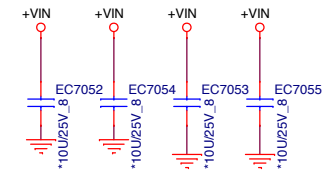
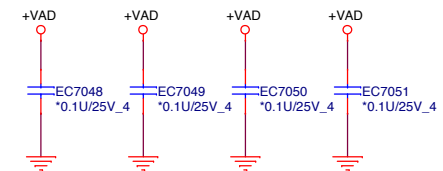
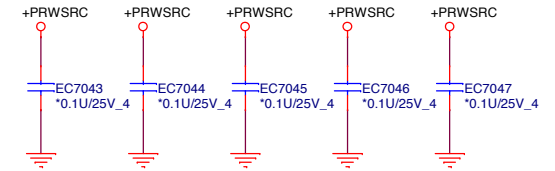
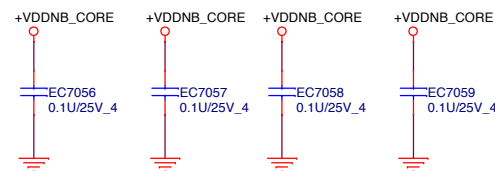
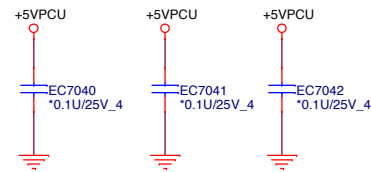
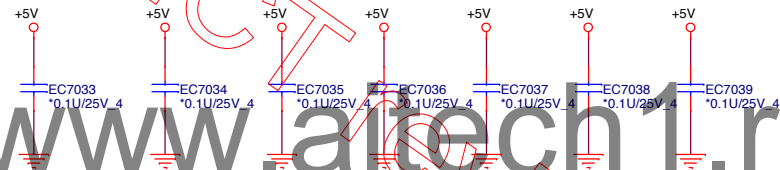
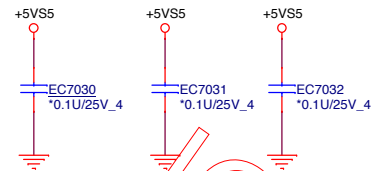
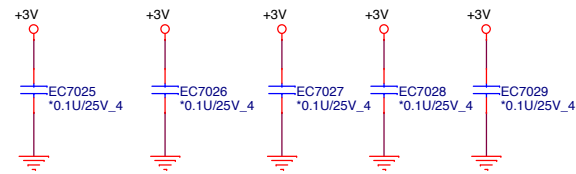
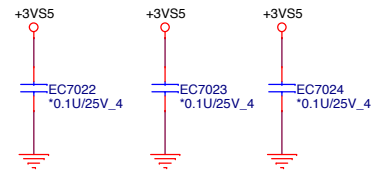
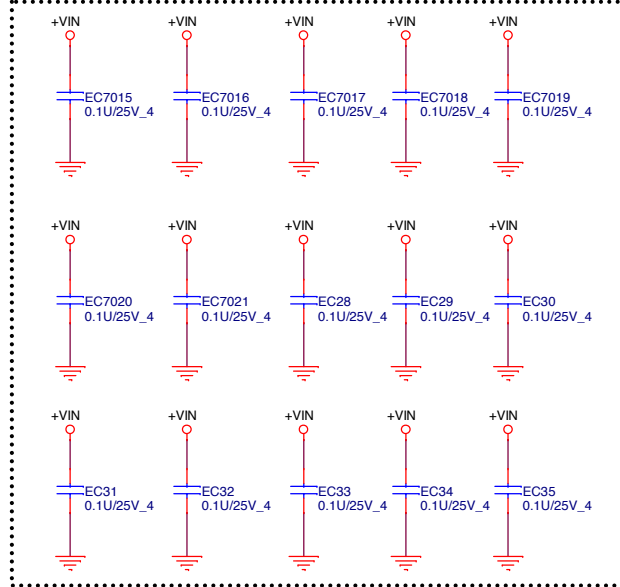


1118 DB modify FP

1118 DB modify FP

EMI CAPs

Place on +VIN Path



4,5,6,7,10,11,20,21,22,23,24,25,26,28,29,35,37,39 +3V

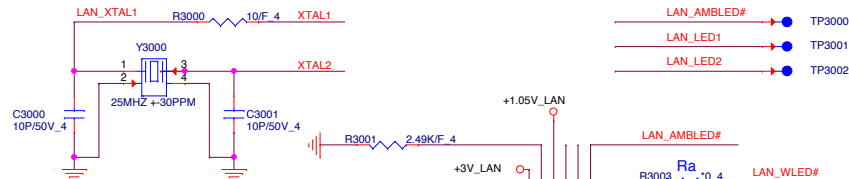
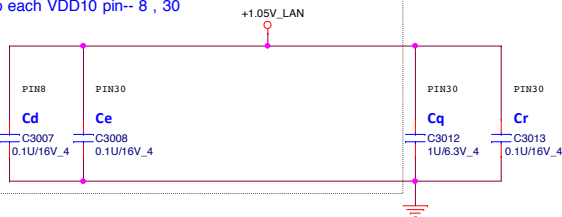


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P8527A

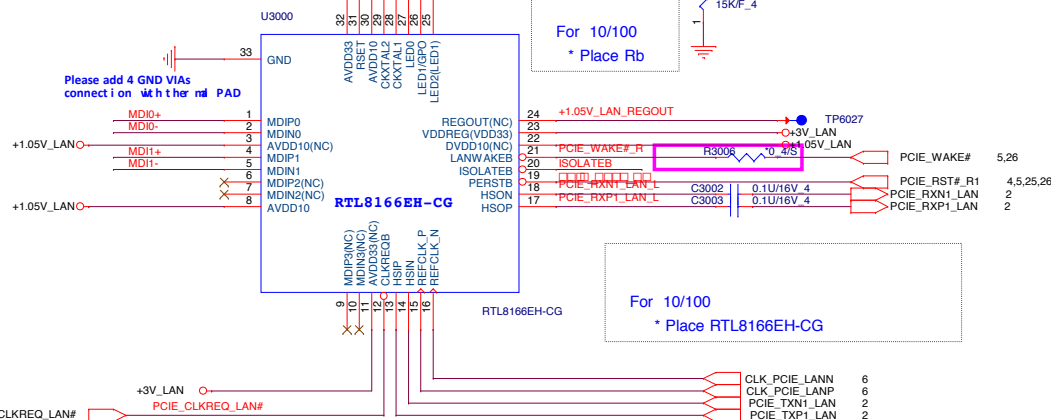
Size	Document Number	Rev
	EMI Cap	
Date: Monday, April 11, 2016	Sheet 27 of 41	

* Place Cq,Cr for RTL8166EH
close to each VDD10 pin-- 30(reserved)

* Place Ce,Cd for RTL8166EH
close to each VDD10 pin-- 8 , 30



```
if ISOLATED pin
pull-low, the LAN
chip will not drive
it's PCI-E outputs
( excluding
PCIE_WAKE# pin )
```

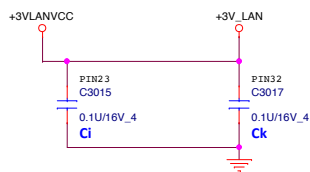


For 10/100

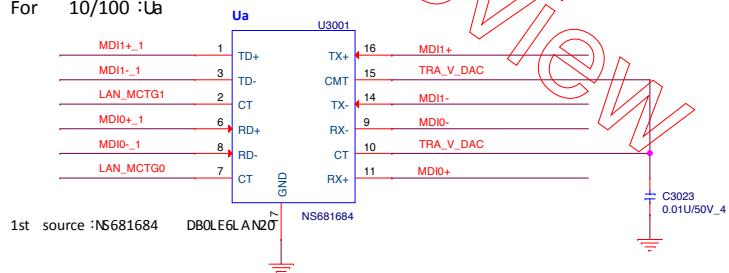
* Place RTL8166EH-CG

Close RJ45

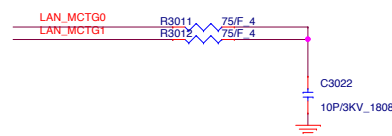
* Place Ci and Ck, close to each VDD33 pin-- 23, 32 for RTL8166EH



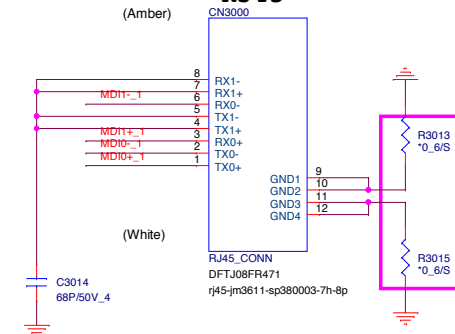
For 10/100 :Ua

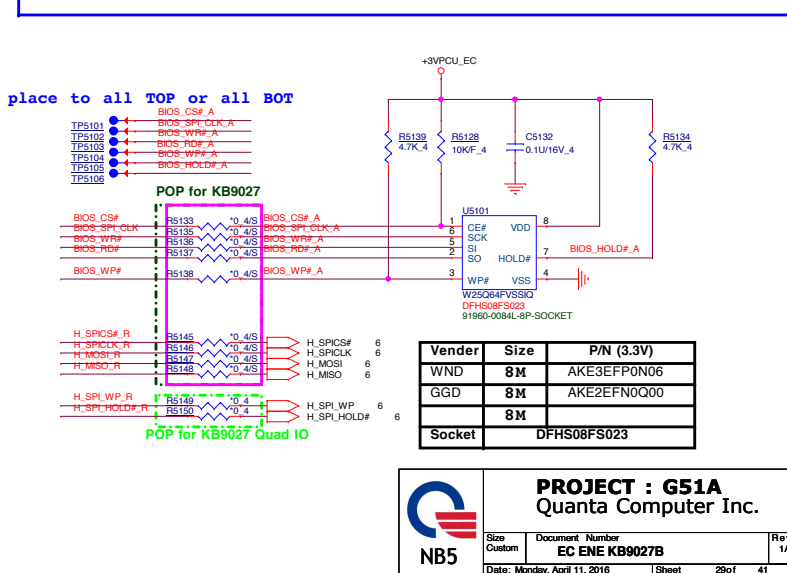
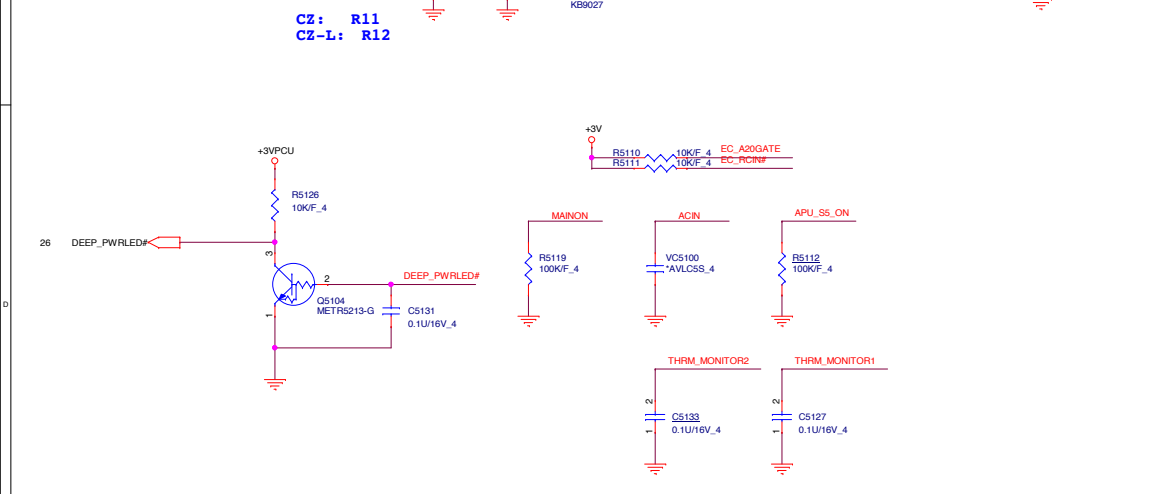


1st source : NS681684

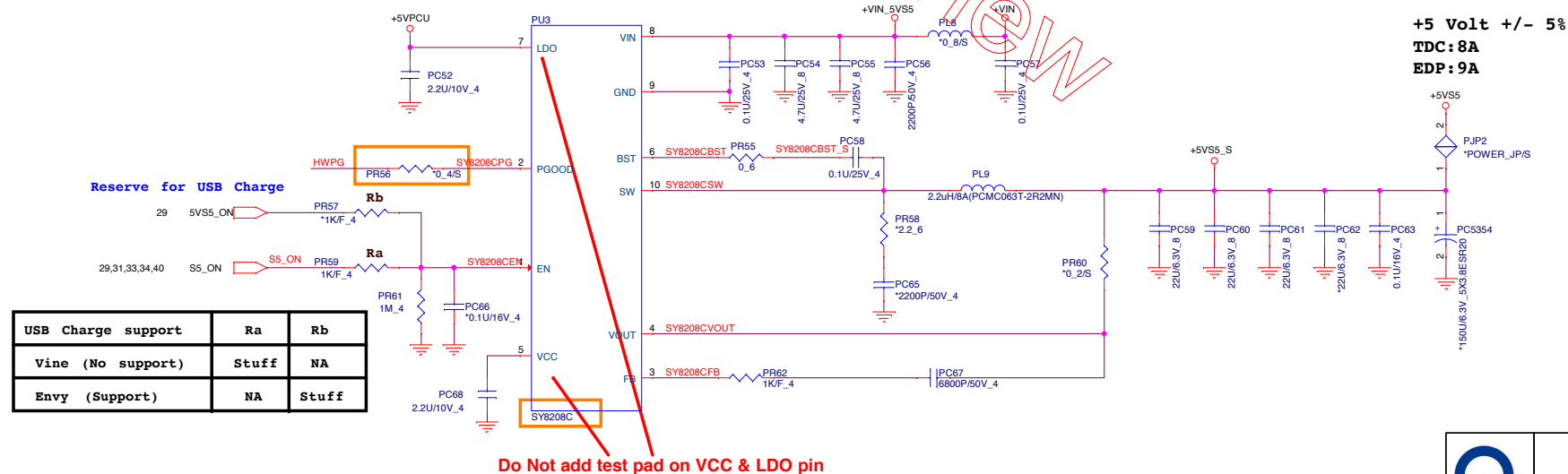
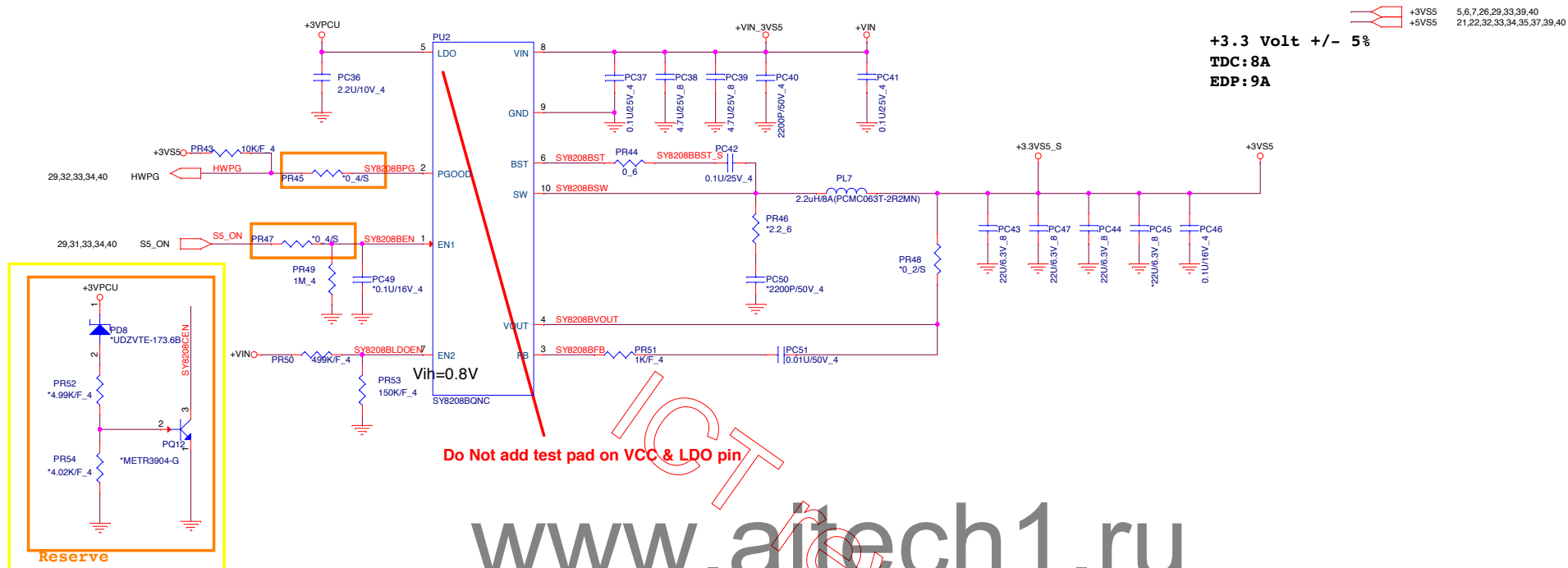


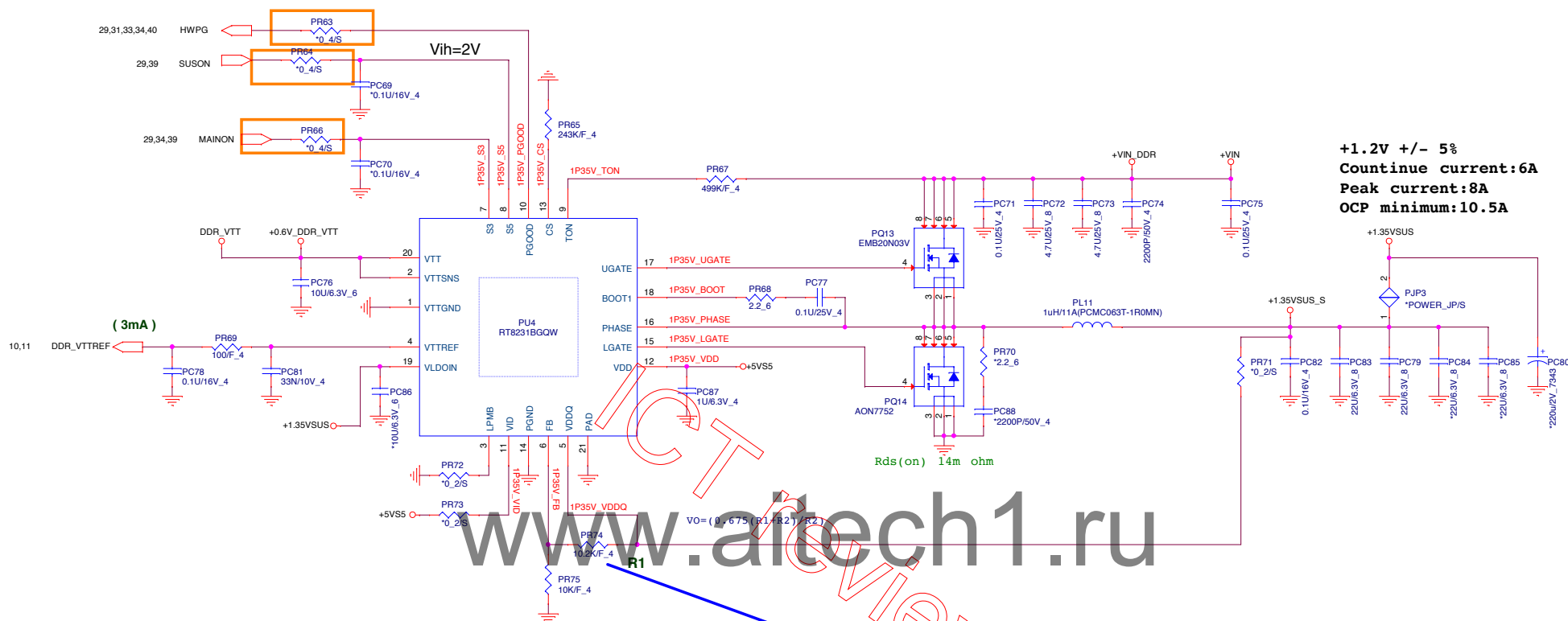
RJ45



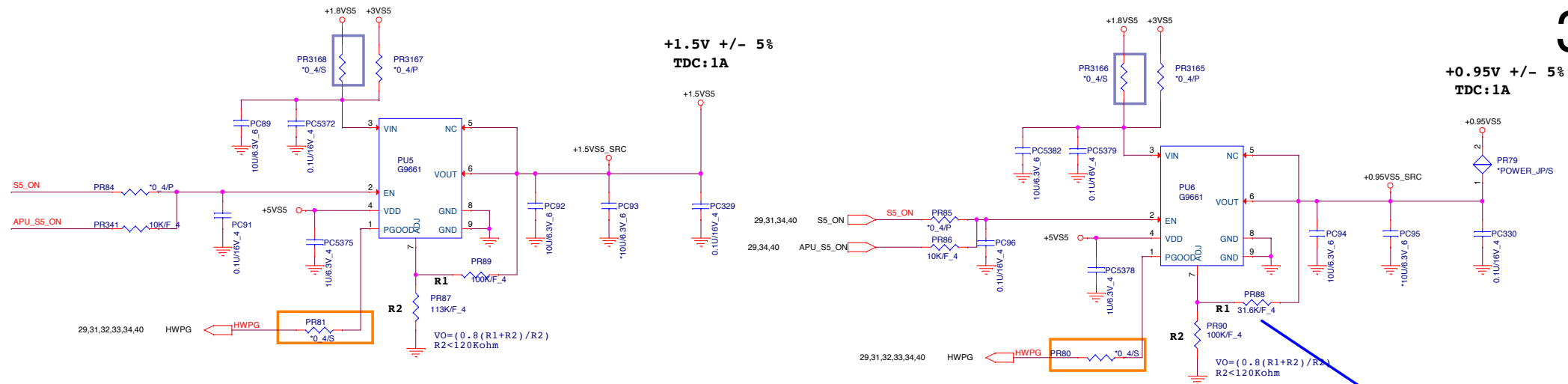


Vender	Size	P/N (3.3V)
WND	8M	AKE3EFP0N06
GGD	8M	AKE2EFN0Q00
	8M	
Socket	DFHS08FS023	

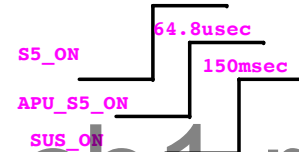




	R1		
DDR3L	10.2K	CS31022FB17	1.35V
DDR4	7.87K	CS27872FB13	1.2V

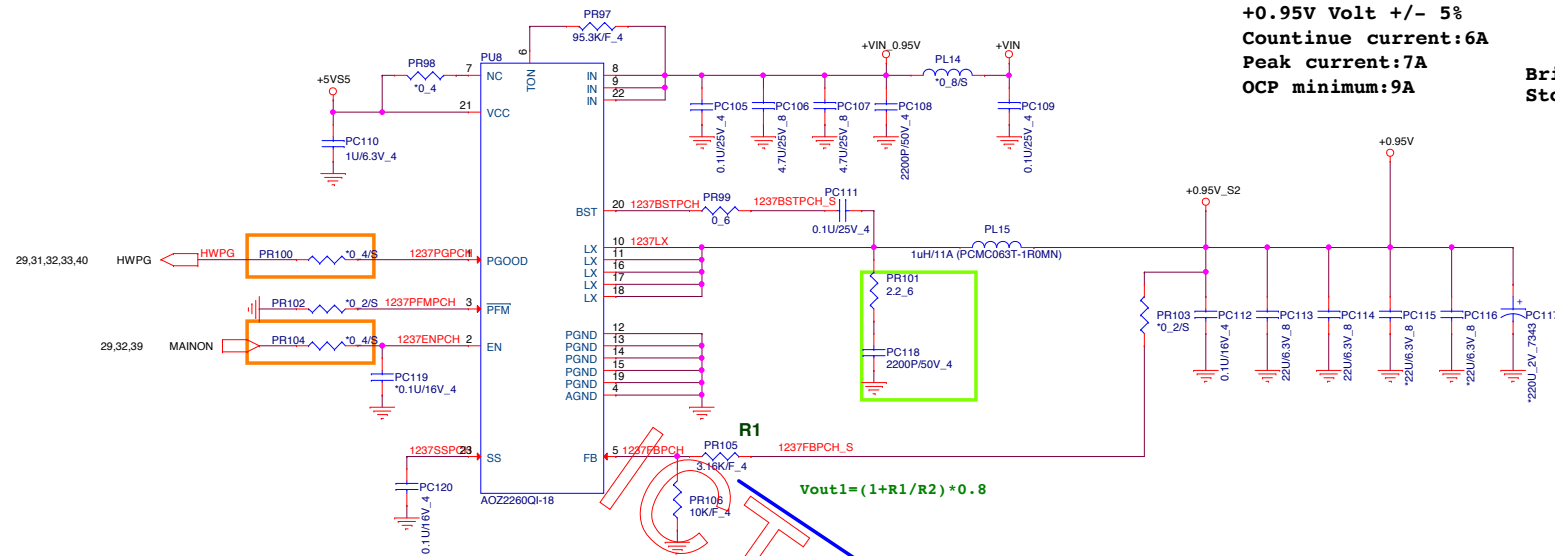


	R1		
Carrizo-L & Stoney	18.7K	CS31872FB19	0.95V
Bristol & Carrizo	31.6K	CS33162FB14	1.05V



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Bristol VDDP=1.05V
 Stoney VDDP=0.95V



+0.95V Volt +/- 5%
Countinue current:6A
Peak current:7A
OCP minimum:9A

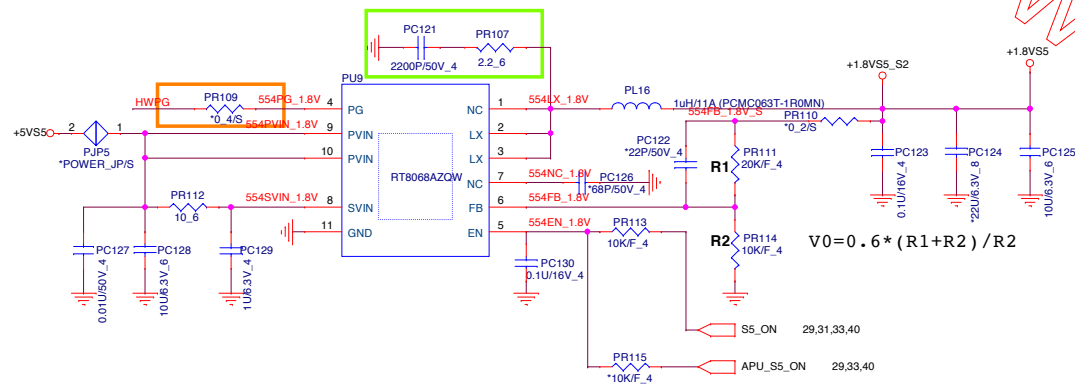
Bristol VDDP=1.05V
Stoney ,CZ&CZ-L VDDP=0.95V

Vo	Rton
0.95V	82k
1V	84.5k
1.05V	95.3k
1.35V	113k
1.5V	127k

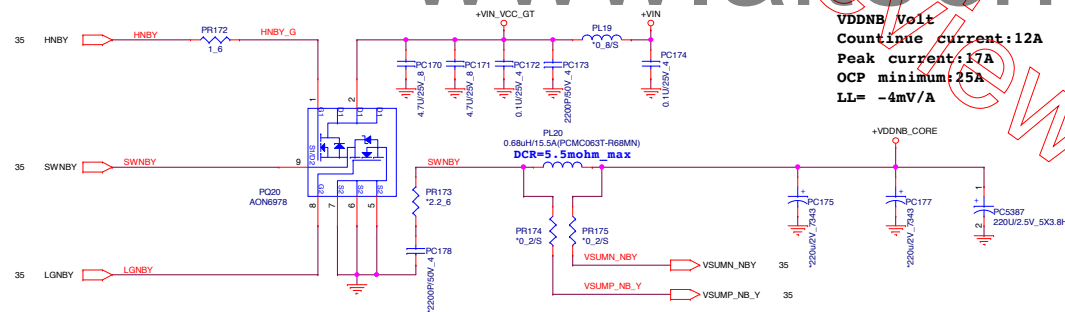
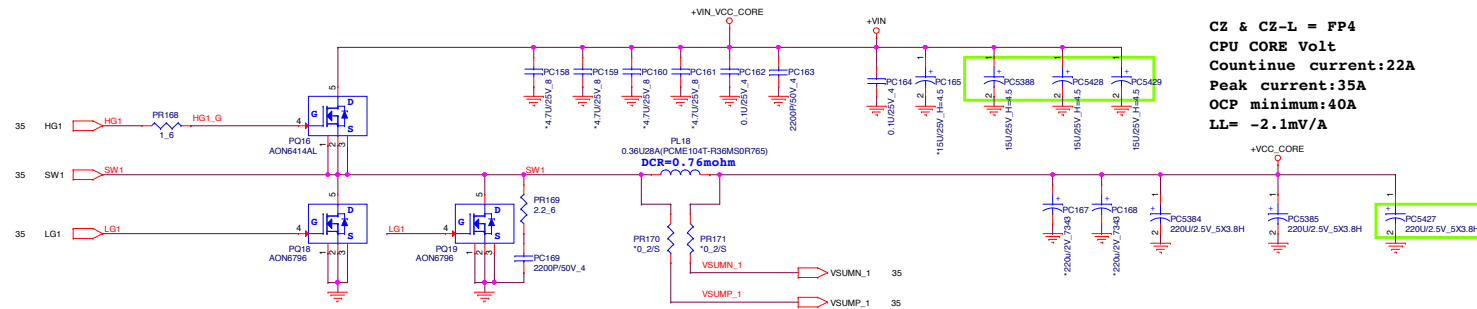
$$V_{out1} = (1 + R1/R2) * 0.8$$

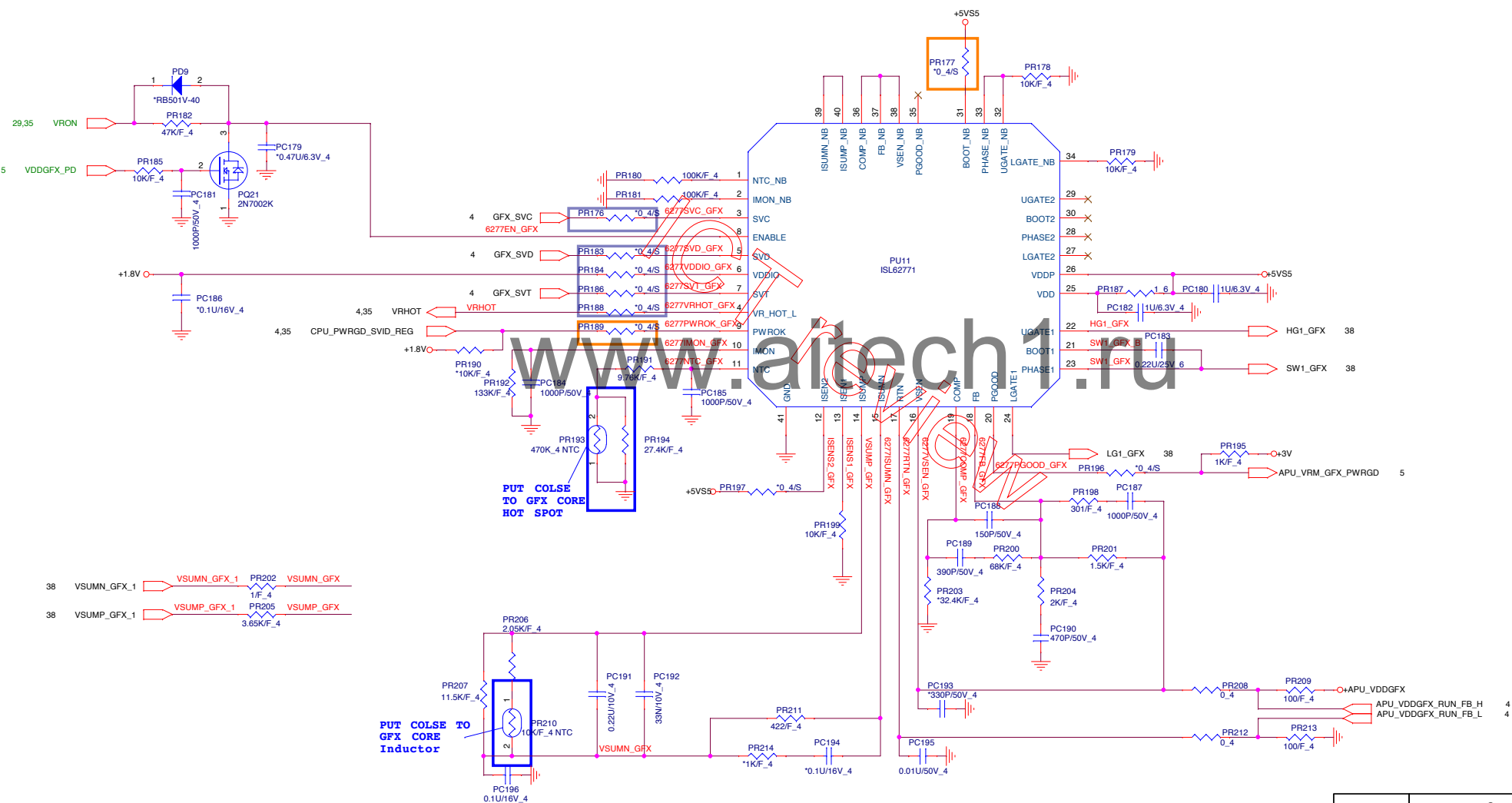
	R1		
Carriazo-L & Stoner	1.91K	CS21912FB13	0.95V
Bristol & Carriazo	3.16K	CS23162FB04	1.05V

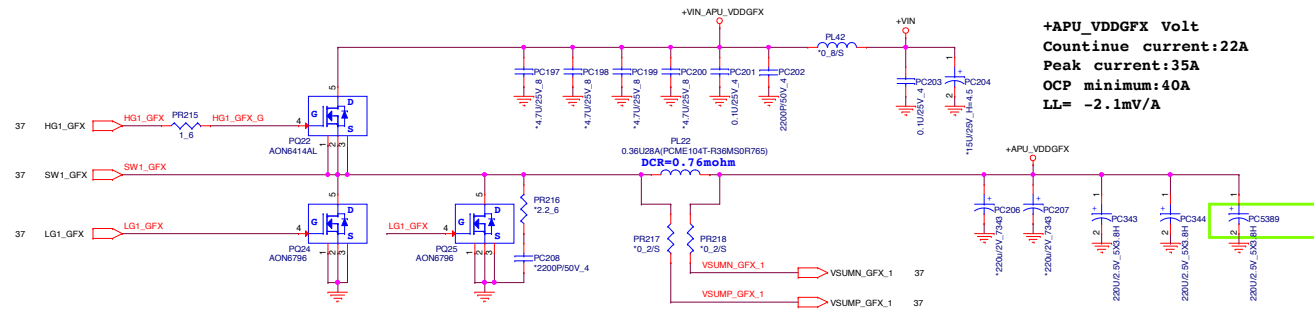
1.8VS5 +/- 3%
TDC: 3A
EDP: 4A



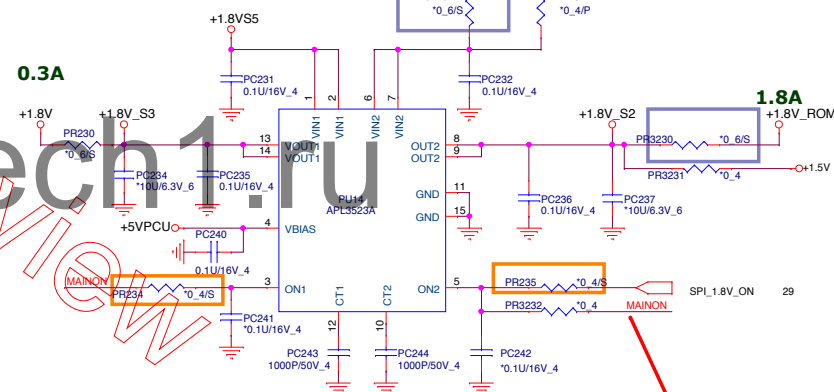
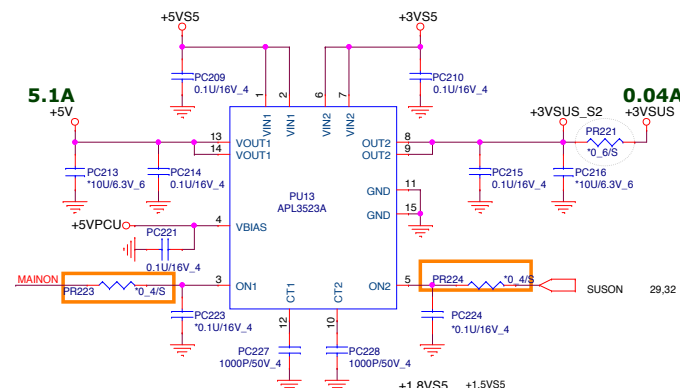
$$V_0 = 0.6 * (R_1 + R_2) / R_2$$



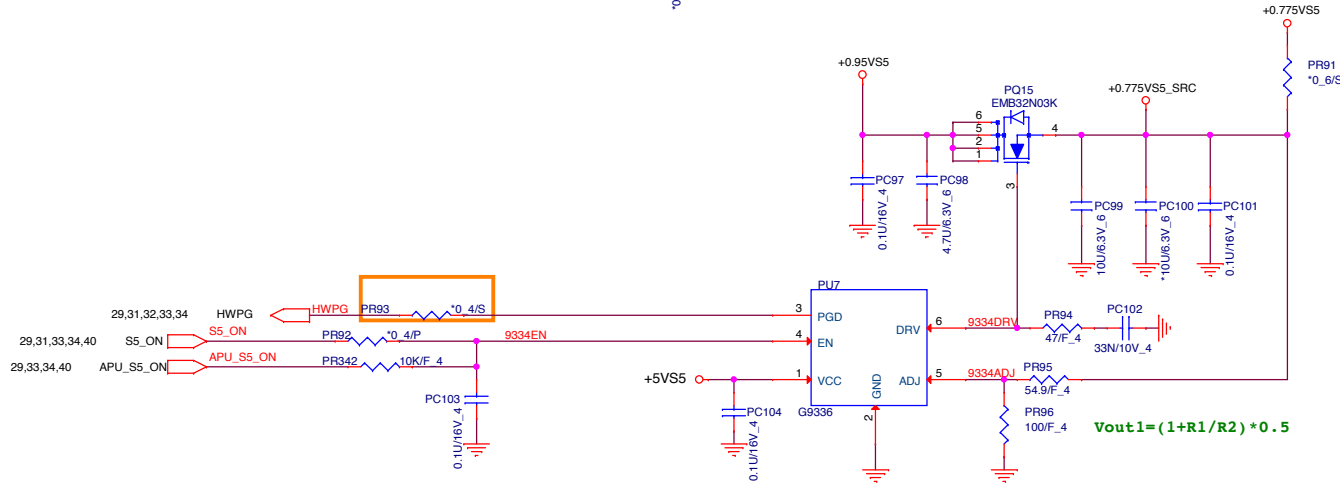
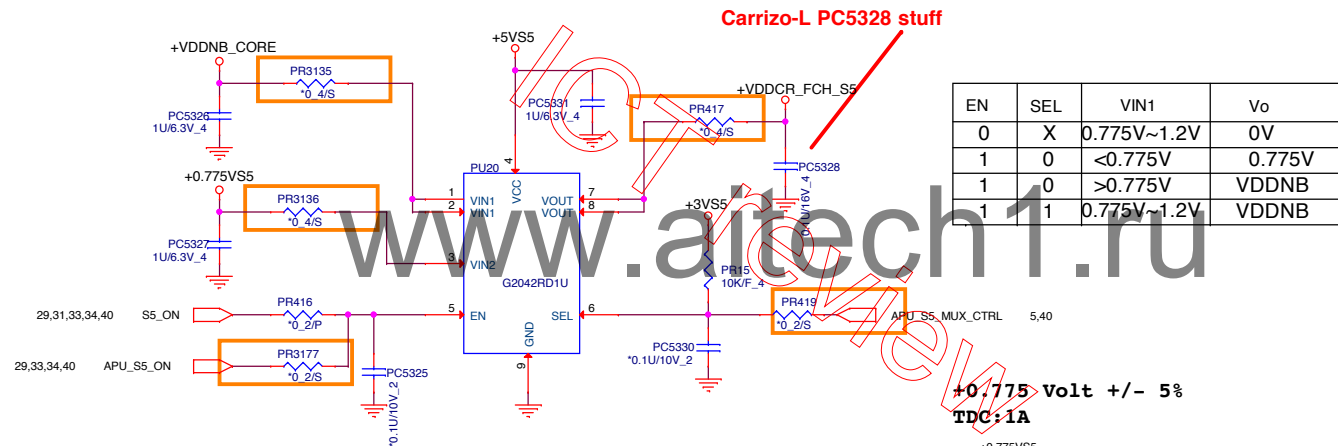
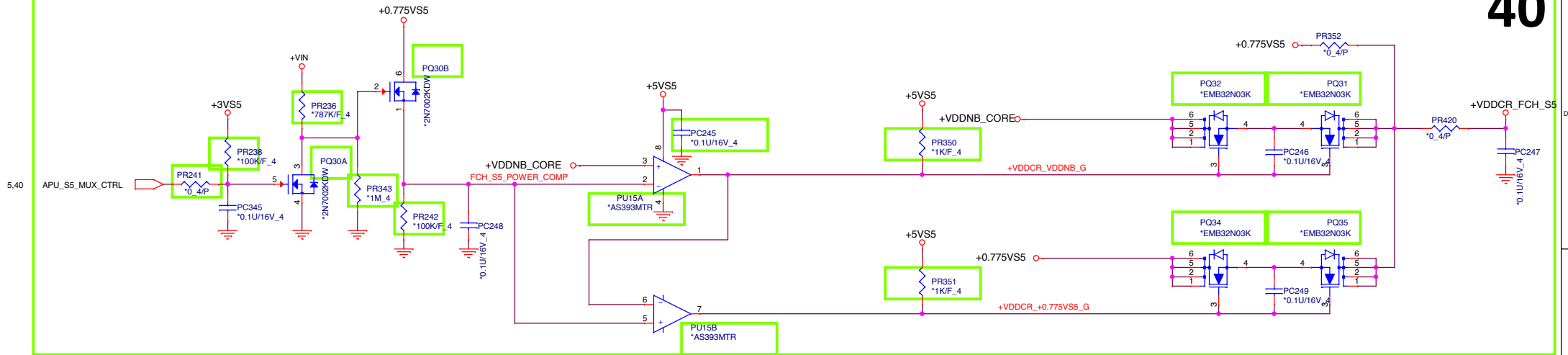




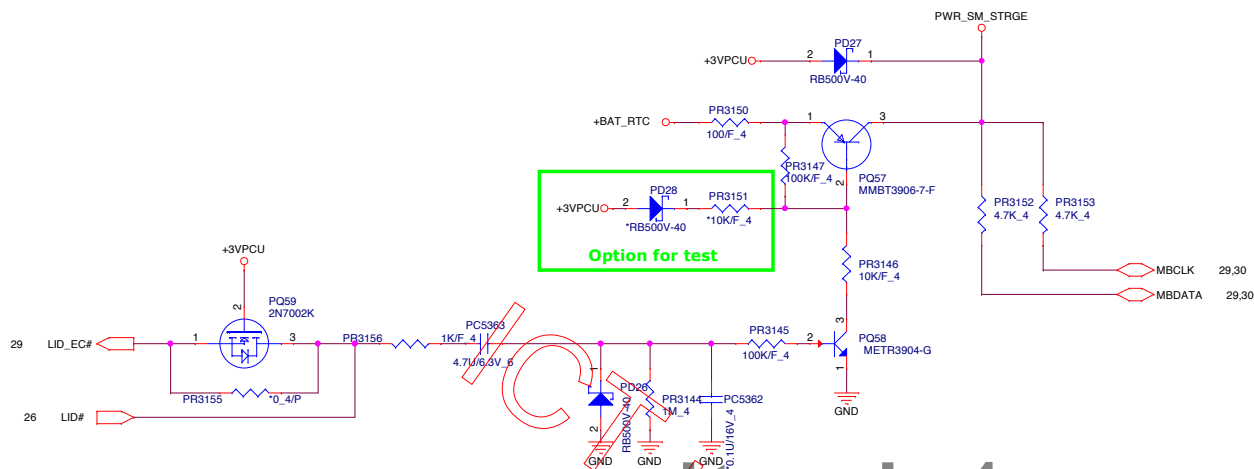
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Carrizo	Stuff PR235 ,PR3230,PR3229
Carrizo-L	stuff PR3232 ,PR3231,PR3227



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